FIG.1

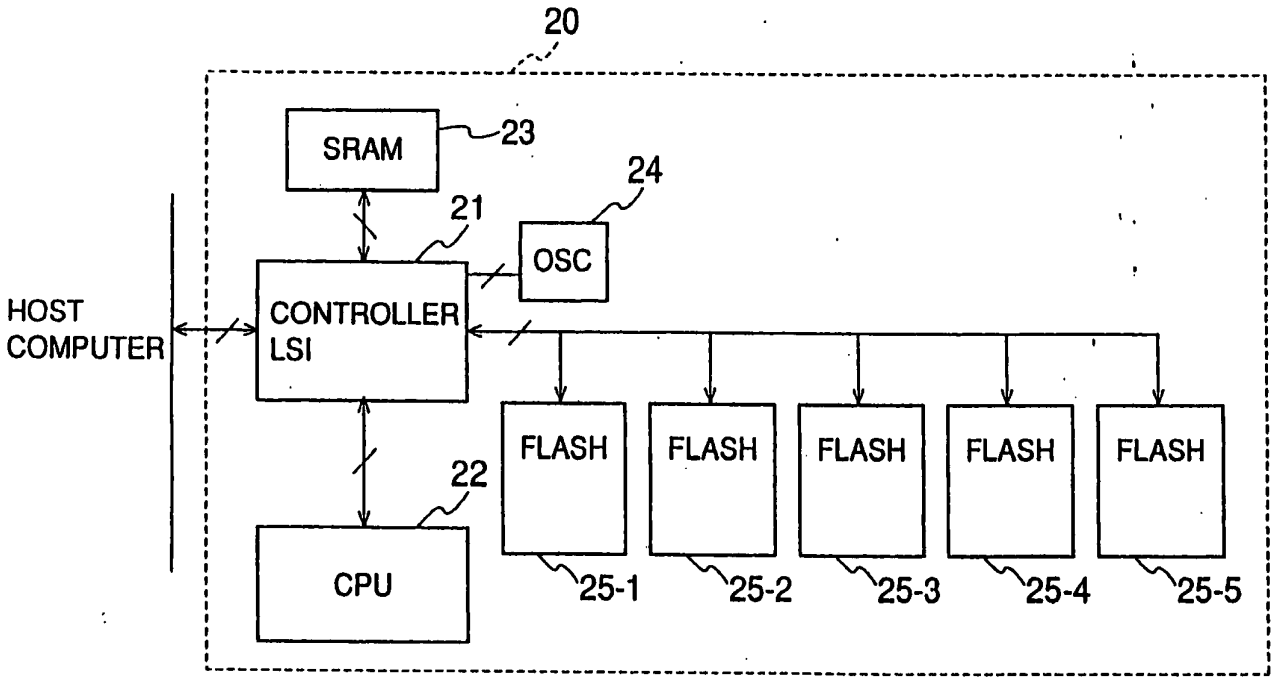

20
SRAM
23
24
21
OSC
HOST
COMPUTER
CONTROLLER
LSI
FLASH
FLASH
FLASH
FLASH
FLASH
22
CPU
25-1
25-2
25-3
25-4
25-5

FIG.2

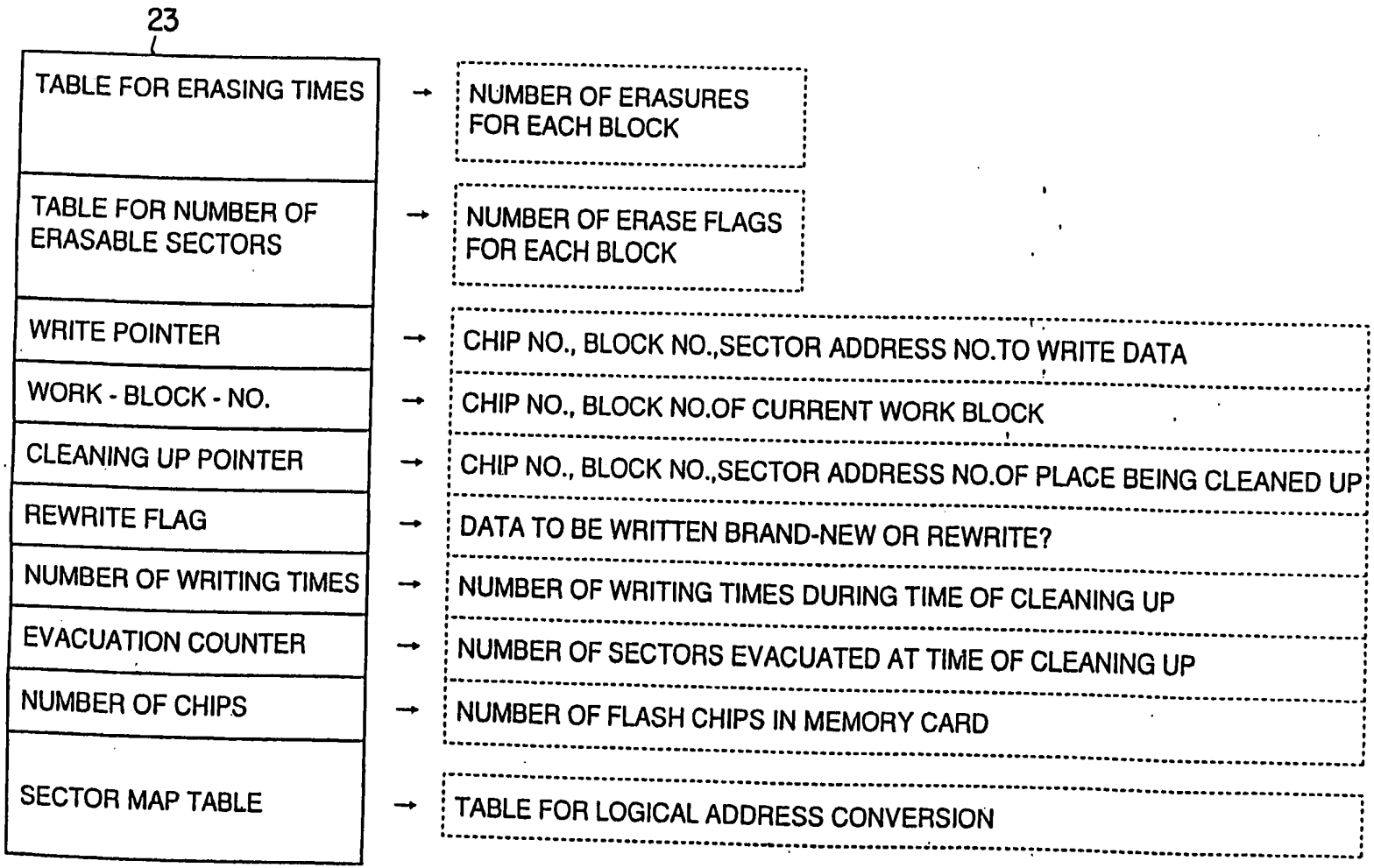

23
TABLE FOR ERASING TIMES
NUMBER OF ERASURES FOR EACH BLOCK
TABLE FOR NUMBER OF ERASABLE SECTORS
NUMBER OF ERASE FLAGS FOR EACH BLOCK
WRITE POINTER
CHIP NO., BLOCK NO.,SECTOR ADDRESS NO.TO WRITE DATA
WORK - BLOCK - NO.
CHIP NO., BLOCK NO.OF CURRENT WORK BLOCK
CLEANING UP POINTER
CHIP NO., BLOCK NO.,SECTOR ADDRESS NO.OF PLACE BEING CLEANED UP
REWRITE FLAG
DATA TO BE WRITTEN BRAND-NEW OR REWRITE?
NUMBER OF WRITING TIMES
NUMBER OF WRITING TIMES DURING TIME OF CLEANING UP
EVACUATION COUNTER
NUMBER OF SECTORS EVACUATED AT TIME OF CLEANING UP
NUMBER OF CHIPS
NUMBER OF FLASH CHIPS IN MEMORY CARD
SECTOR MAP TABLE
TABLE FOR LOGICAL ADDRESS CONVERSION

FIG.3

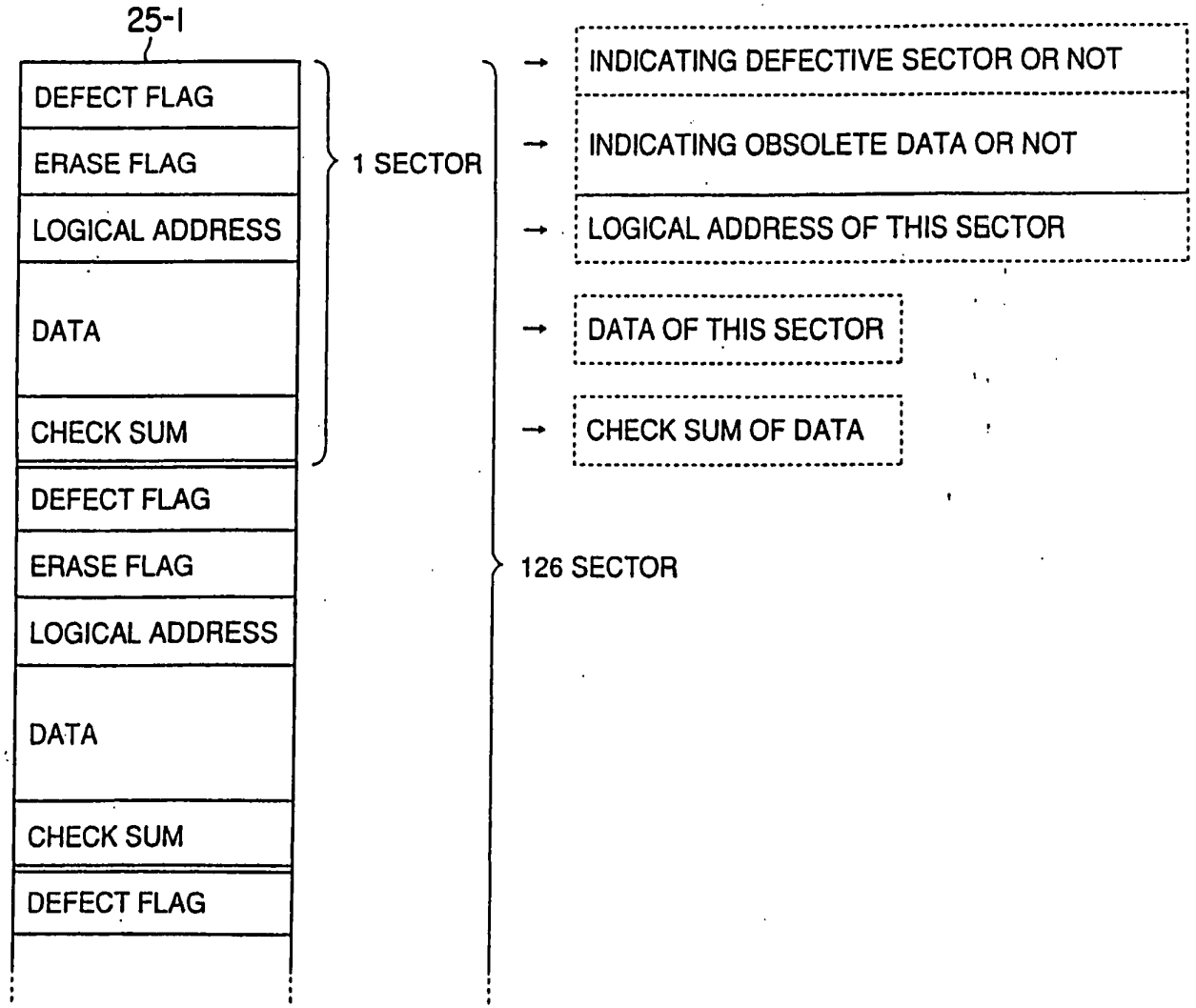

25-1
DEFECT FLAG
ERASE FLAG
LOGICAL ADDRESS
DATA
CHECK SUM
1 SECTOR
DEFECT FLAG
ERASE FLAG
LOGICAL ADDRESS
DATA
CHECK SUM
DEFECT FLAG
INDICATING DEFECTIVE SECTOR OR NOT
INDICATING OBSOLETE DATA OR NOT
LOGICAL ADDRESS OF THIS SECTOR
DATA OF THIS SECTOR
CHECK SUM OF DATA
126 SECTOR

FIG.4

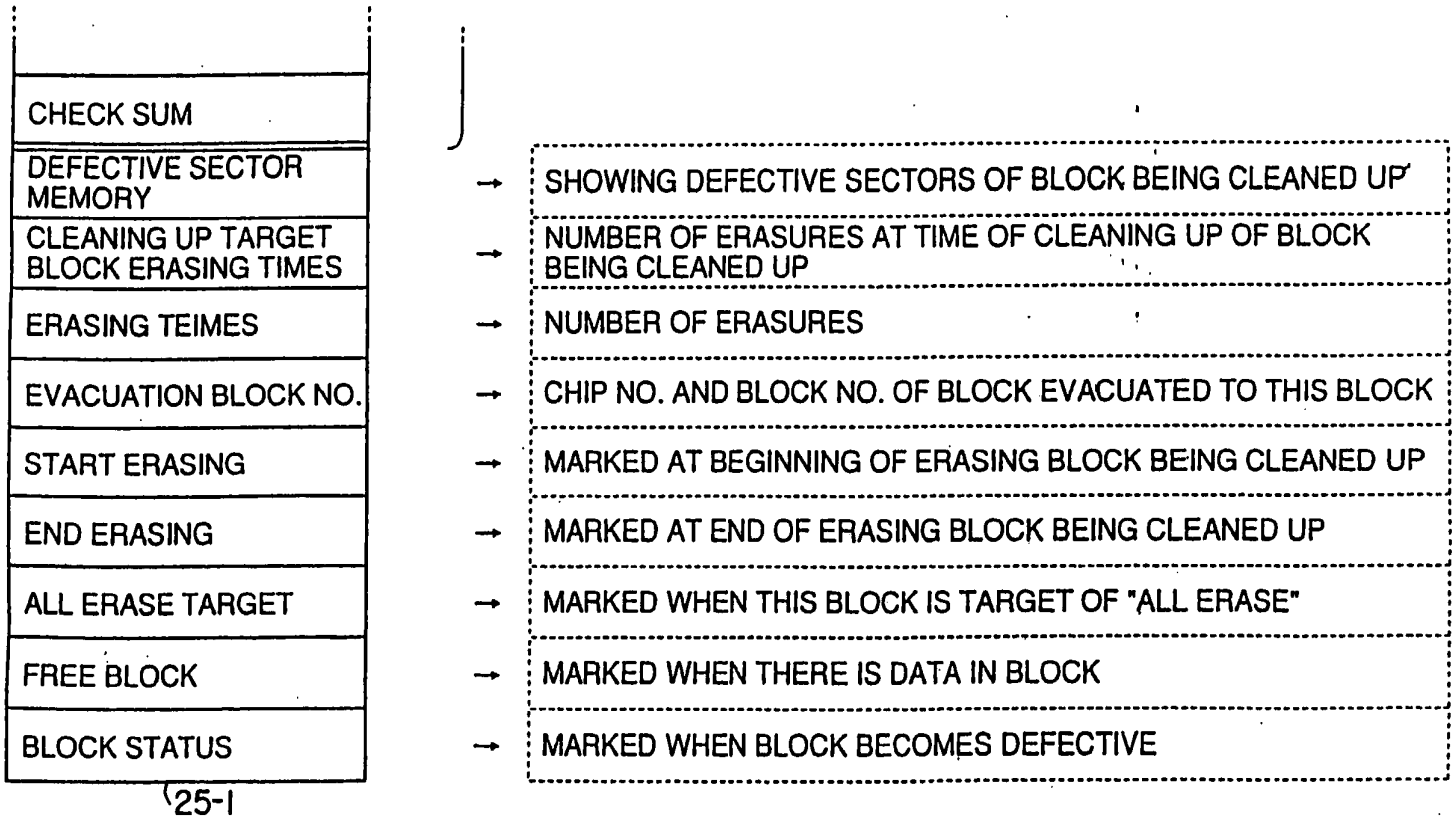

CHECK SUM
DEFECTIVE SECTOR MEMORY
CLEANING UP TARGET BLOCK ERASING TIMES
ERASING TEIMES
EVACUATION BLOCK NO.
START ERASING
END ERASING
ALL ERASE TARGET
FREE BLOCK
BLOCK STATUS
25-1
SHOWING DEFECTIVE SECTORS OF BLOCK BEING CLEANED UP
NUMBER OF ERASURES AT TIME OF CLEANING UP OF BLOCK BEING CLEANED UP
NUMBER OF ERASURES
CHIP NO. AND BLOCK NO. OF BLOCK EVACUATED TO THIS BLOCK
MARKED AT BEGINNING OF ERASING BLOCK BEING CLEANED UP
MARKED AT END OF ERASING BLOCK BEING CLEANED UP
MARKED WHEN THIS BLOCK IS TARGET OF "ALL ERASE"
MARKED WHEN THERE IS DATA IN BLOCK
MARKED WHEN BLOCK BECOMES DEFECTIVE

FIG.5

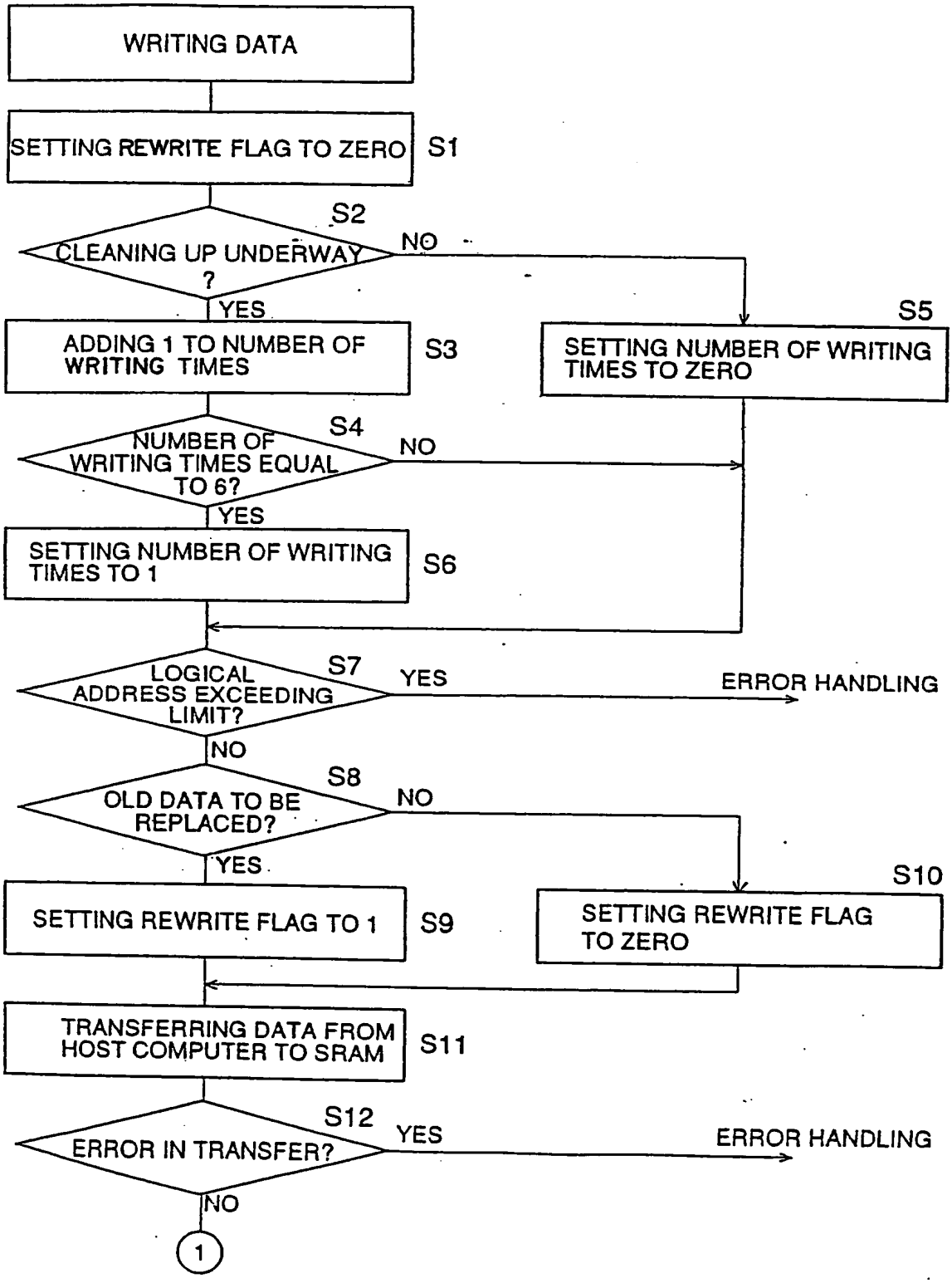

WRITING DATA
SETTING REWRITE FLAG TO ZERO
S1
S2
CLEANING UP UNDERWAY ?
NO
YES
ADDING 1 TO NUMBER OF WRITING TIMES
S3
S5
SETTING NUMBER OF WRITING TIMES TO ZERO
S4
NUMBER OF WRITING TIMES EQUAL TO 6?
NO
YES
SETTING NUMBER OF WRITING TIMES TO 1
S6
S7
LOGICAL ADDRESS EXCEEDING LIMIT?
YES
ERROR HANDLING
NO
S8
OLD DATA TO BE REPLACED?
NO
YES
S10
SETTING REWRITE FLAG TO 1
S9
SETTING REWRITE FLAG TO ZERO
TRANSFERRING DATA FROM HOST COMPUTER TO SRAM
S11
S12
ERROR IN TRANSFER?
YES
ERROR HANDLING
NO
1

FIG.6

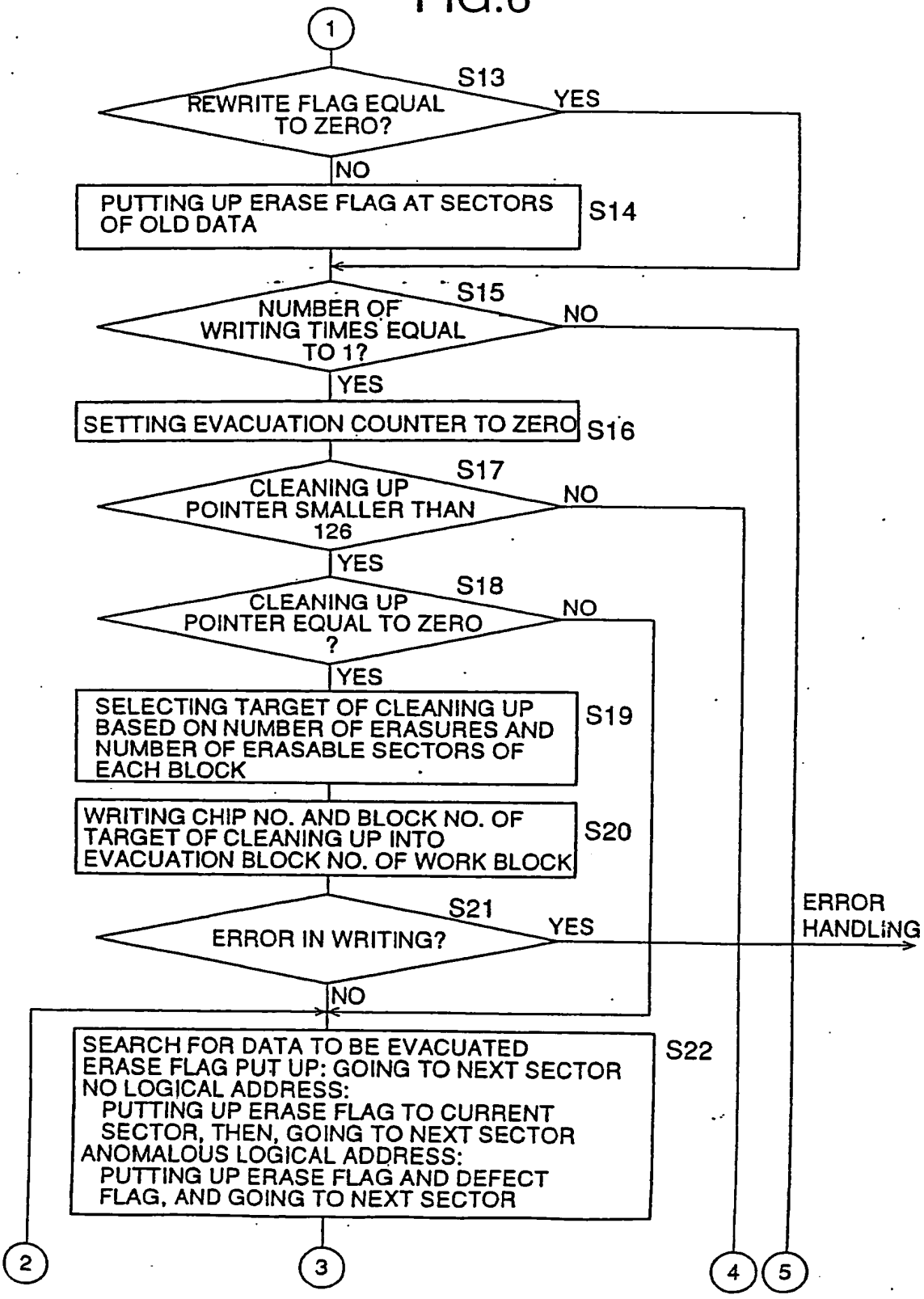

1
S13
REWRITE FLAG EQUAL TO ZERO?
YES
NO
PUTTING UP ERASE FLAG AT SECTORS OF OLD DATA
S14
S15
NUMBER OF WRITING TIMES EQUAL TO 1?
NO
YES
SETTING EVACUATION COUNTER TO ZERO
S16
S17
CLEANING UP POINTER SMALLER THAN 126
NO
YES
S18
CLEANING UP POINTER EQUAL TO ZERO ?
NO
YES
SELECTING TARGET OF CLEANING UP BASED ON NUMBER OF ERASURES AND NUMBER OF ERASABLE SECTORS OF EACH BLOCK
S19
WRITING CHIP NO. AND BLOCK NO. OF TARGET OF CLEANING UP INTO EVACUATION BLOCK NO. OF WORK BLOCK
S20
S21
ERROR IN WRITING?
YES
ERROR HANDLING
NO
SEARCH FOR DATA TO BE EVACUATED
ERASE FLAG PUT UP: GOING TO NEXT SECTOR
NO LOGICAL ADDRESS:
PUTTING UP ERASE FLAG TO CURRENT SECTOR, THEN, GOING TO NEXT SECTOR
ANOMALOUS LOGICAL ADDRESS:
PUTTING UP ERASE FLAG AND DEFECT FLAG, AND GOING TO NEXT SECTOR
S22
2
3
4
5

FIG.7

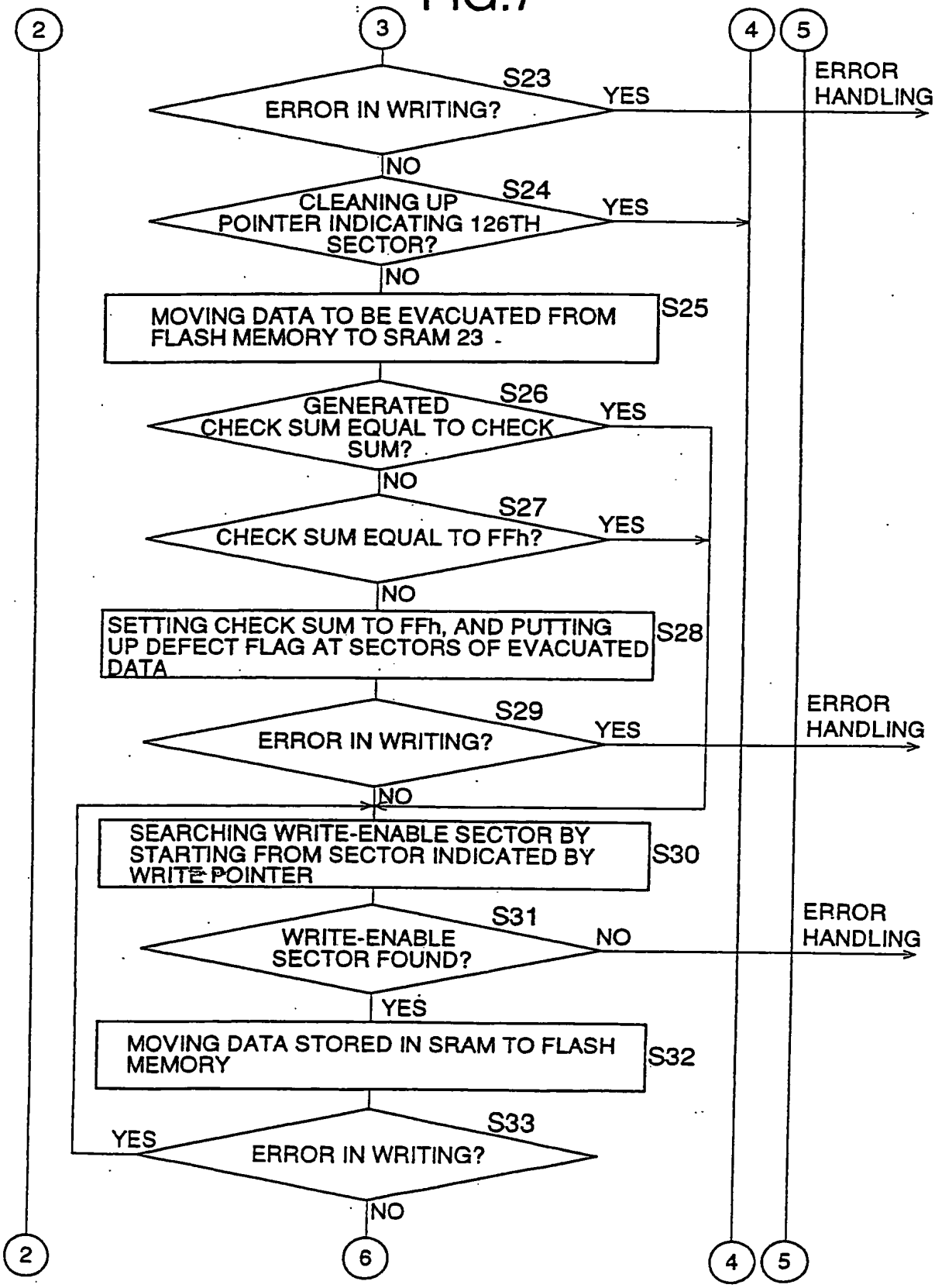

2
3
4
5
S23
ERROR IN WRITING?
YES
ERROR HANDLING
NO
S24
CLEANING UP POINTER INDICATING 126TH SECTOR?
YES
NO
MOVING DATA TO BE EVACUATED FROM FLASH MEMORY TO SRAM 23
S25
S26
GENERATED CHECK SUM EQUAL TO CHECK SUM?
YES
NO
S27
CHECK SUM EQUAL TO FFh?
YES
NO
SETTING CHECK SUM TO FFh, AND PUTTING UP DEFECT FLAG AT SECTORS OF EVACUATED DATA
S28
S29
ERROR IN WRITING?
YES
ERROR HANDLING
NO
SEARCHING WRITE-ENABLE SECTOR BY STARTING FROM SECTOR INDICATED BY WRITE POINTER
S30
S31
WRITE-ENABLE SECTOR FOUND?
NO
ERROR HANDLING
YES
MOVING DATA STORED IN SRAM TO FLASH MEMORY
S32
S33
YES
ERROR IN WRITING?
NO
2
6
4
5

FIG.8

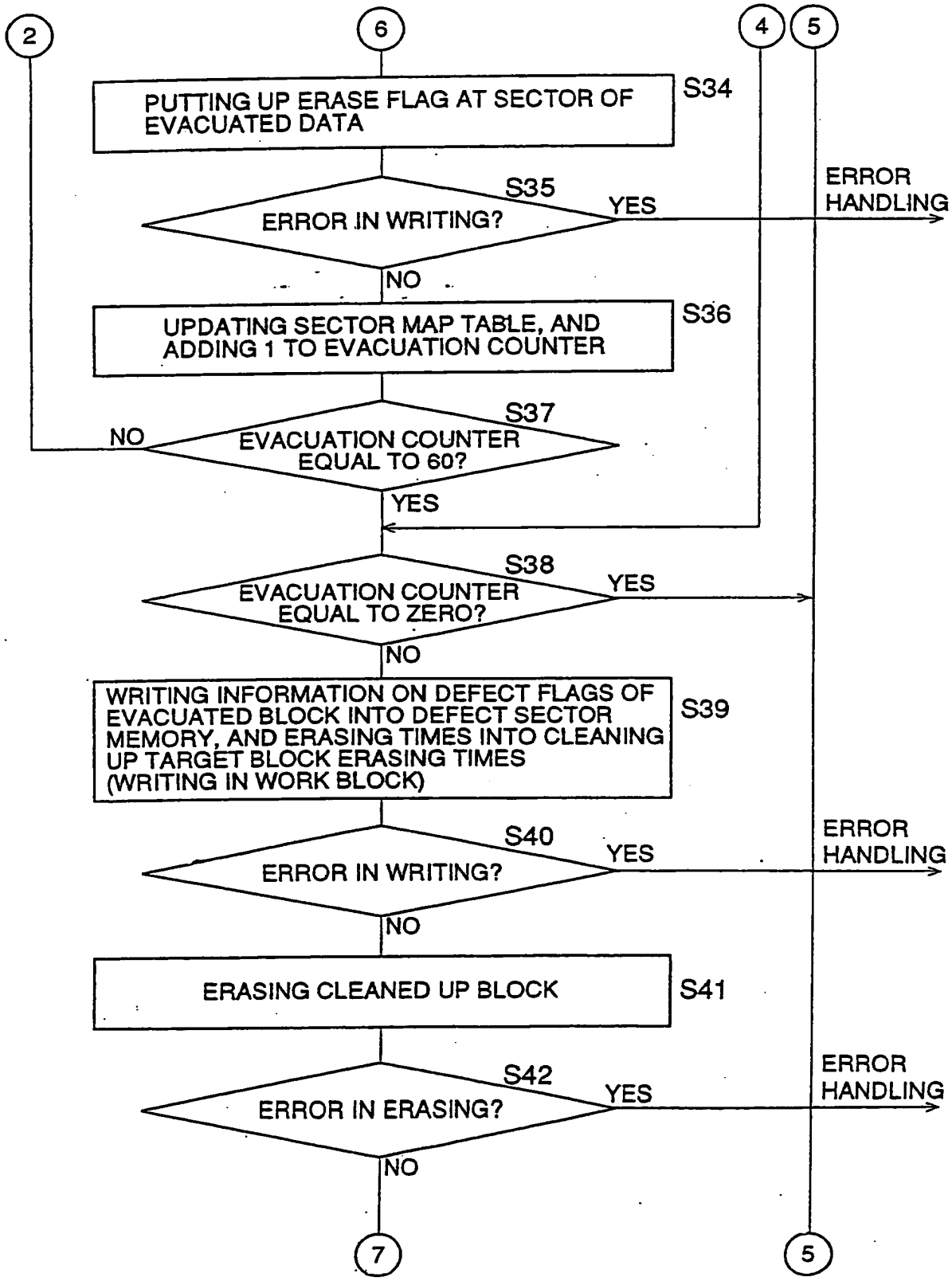

2
6
4
5
PUTTING UP ERASE FLAG AT SECTOR OF EVACUATED DATA
S34
S35
ERROR IN WRITING?
YES
ERROR HANDLING
NO
UPDATING SECTOR MAP TABLE, AND ADDING 1 TO EVACUATION COUNTER
S36
S37
NO
EVACUATION COUNTER EQUAL TO 60?
YES
S38
EVACUATION COUNTER EQUAL TO ZERO?
YES
NO
WRITING INFORMATION ON DEFECT FLAGS OF EVACUATED BLOCK INTO DEFECT SECTOR MEMORY, AND ERASING TIMES INTO CLEANING UP TARGET BLOCK ERASING TIMES (WRITING IN WORK BLOCK)
S39
S40
ERROR IN WRITING?
YES
ERROR HANDLING
NO
ERASING CLEANED UP BLOCK
S41
S42
ERROR IN ERASING?
YES
ERROR HANDLING
NO
7
5

FIG.9

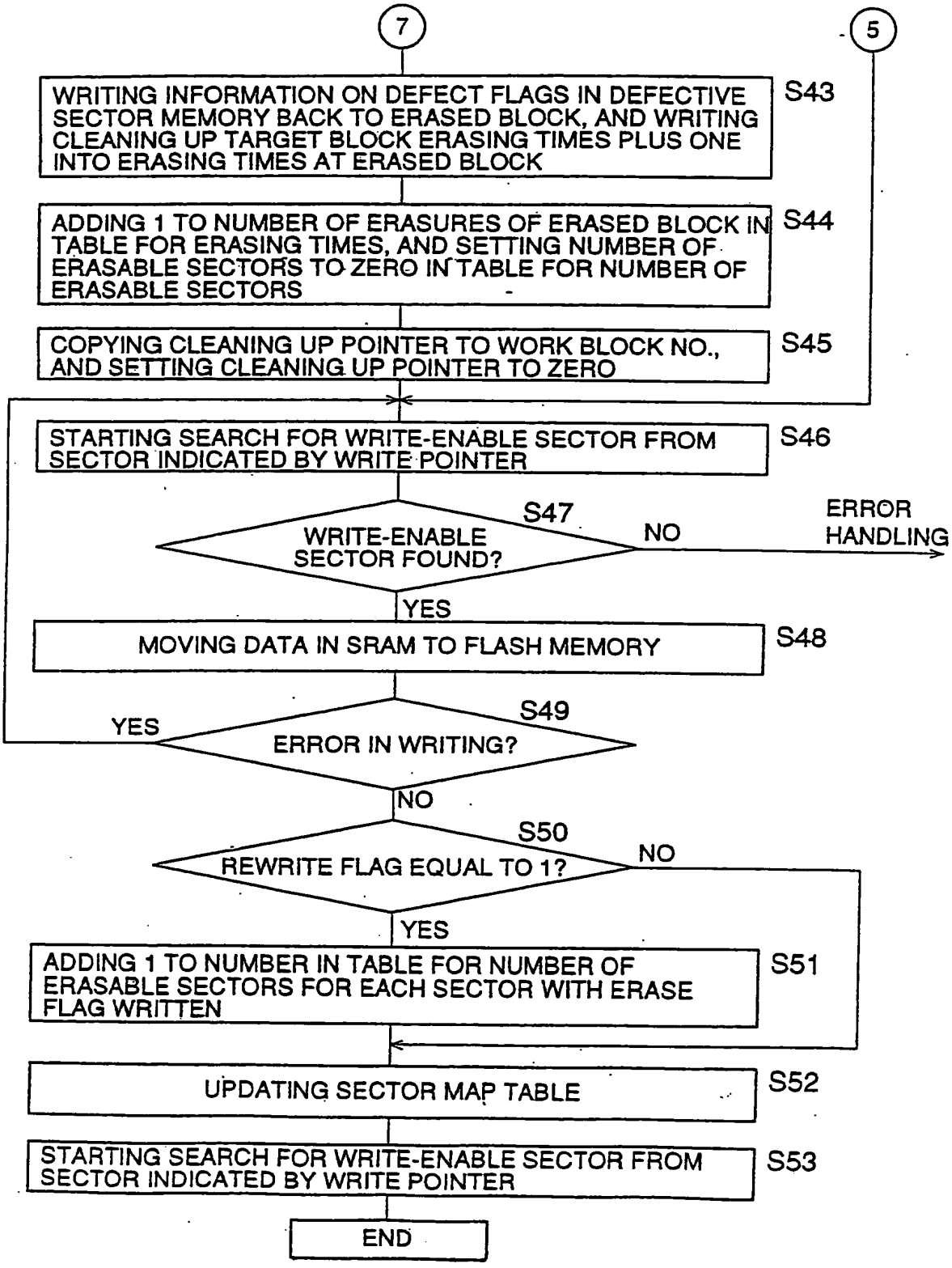

7
5
WRITING INFORMATION ON DEFECT FLAGS IN DEFECTIVE SECTOR MEMORY BACK TO ERASED BLOCK, AND WRITING CLEANING UP TARGET BLOCK ERASING TIMES PLUS ONE INTO ERASING TIMES AT ERASED BLOCK
S43
ADDING 1 TO NUMBER OF ERASURES OF ERASED BLOCK IN TABLE FOR ERASING TIMES, AND SETTING NUMBER OF ERASABLE SECTORS TO ZERO IN TABLE FOR NUMBER OF ERASABLE SECTORS
S44
COPYING CLEANING UP POINTER TO WORK BLOCK NO., AND SETTING CLEANING UP POINTER TO ZERO
S45
STARTING SEARCH FOR WRITE-ENABLE SECTOR FROM SECTOR INDICATED BY WRITE POINTER
S46
S47
WRITE-ENABLE SECTOR FOUND?
NO
ERROR HANDLING
YES
MOVING DATA IN SRAM TO FLASH MEMORY
S48
S49
YES
ERROR IN WRITING?
NO
S50
REWRITE FLAG EQUAL TO 1?
NO
YES
ADDING 1 TO NUMBER IN TABLE FOR NUMBER OF ERASABLE SECTORS FOR EACH SECTOR WITH ERASE FLAG WRITTEN
S51
UPDATING SECTOR MAP TABLE
S52
STARTING SEARCH FOR WRITE-ENABLE SECTOR FROM SECTOR INDICATED BY WRITE POINTER
S53
END

FIG.10A

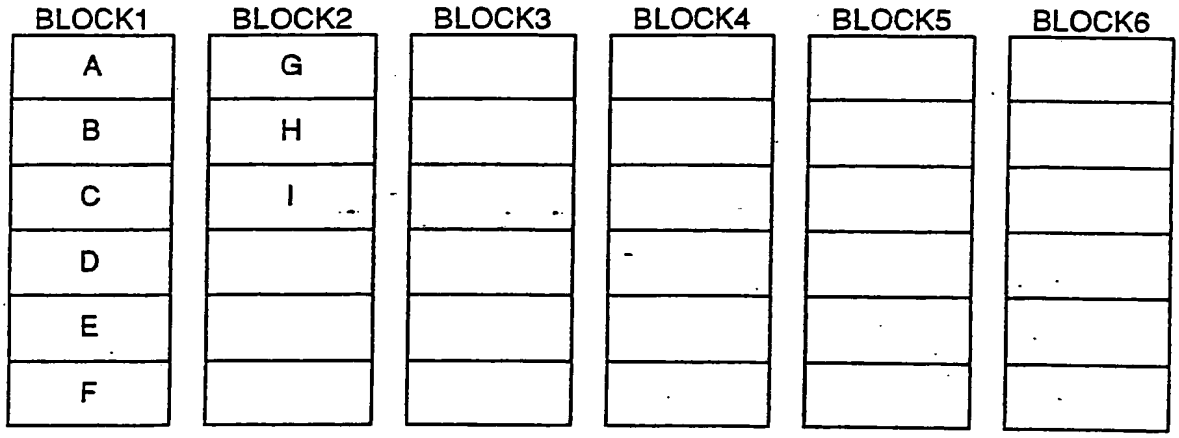


FIG.10B

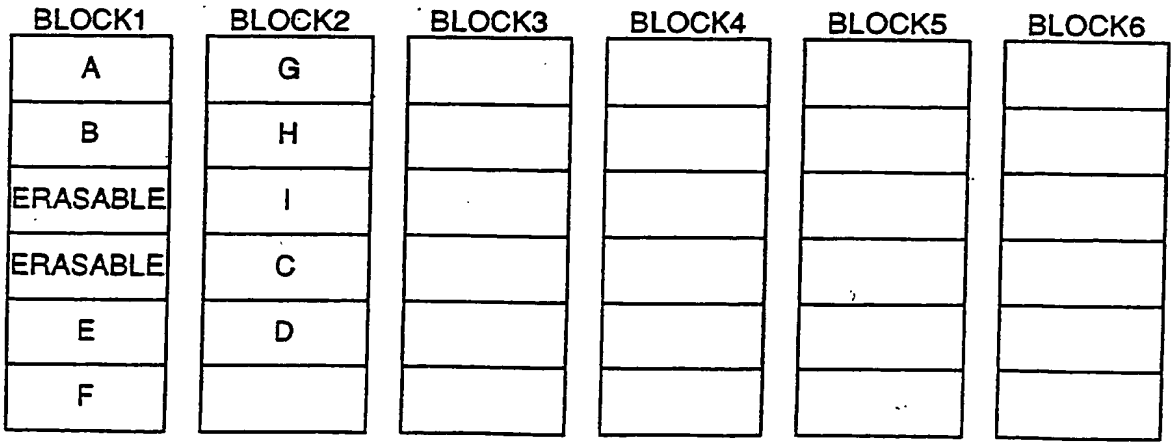


FIG.10C

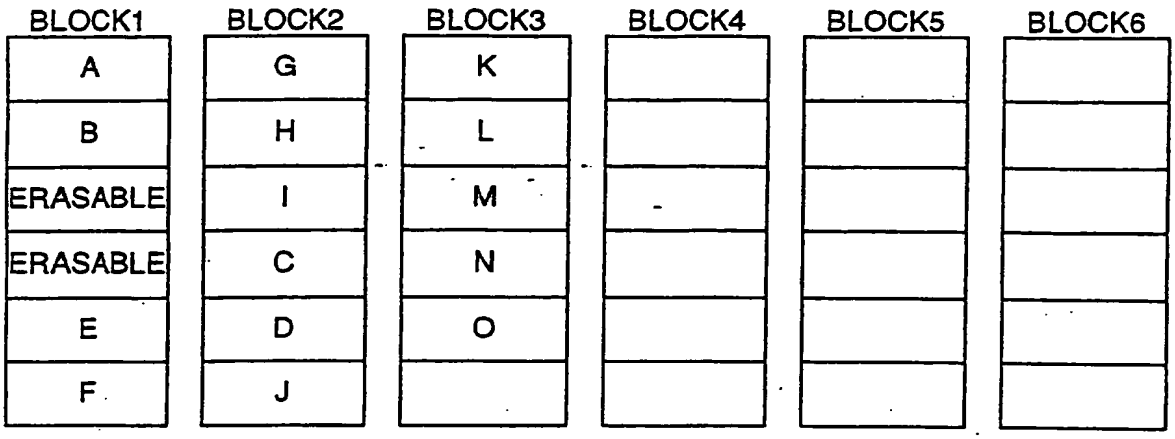


FIG.10D

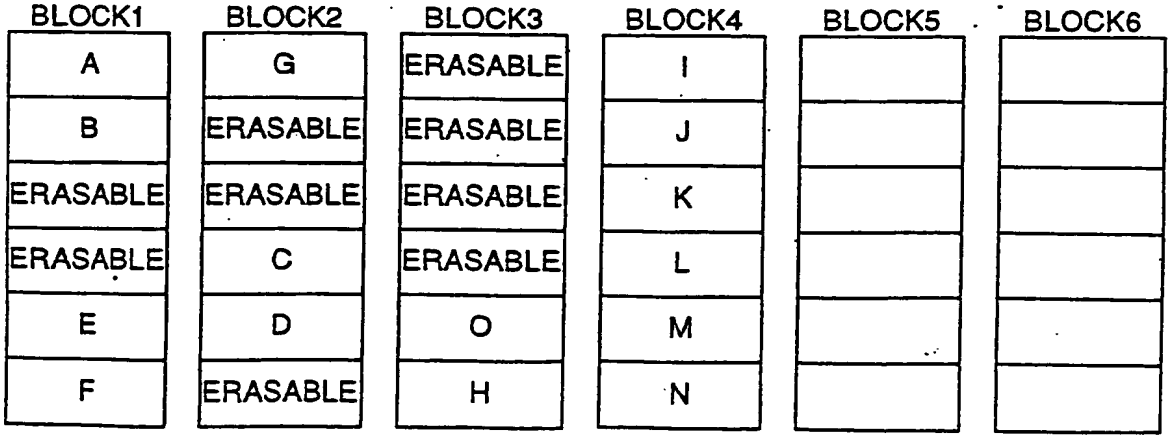


FIG.10E

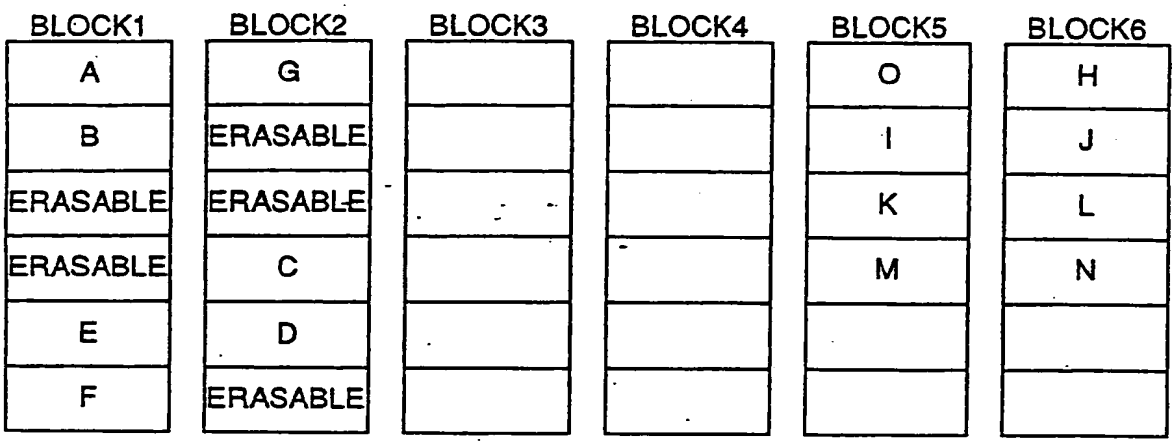


FIG.10F

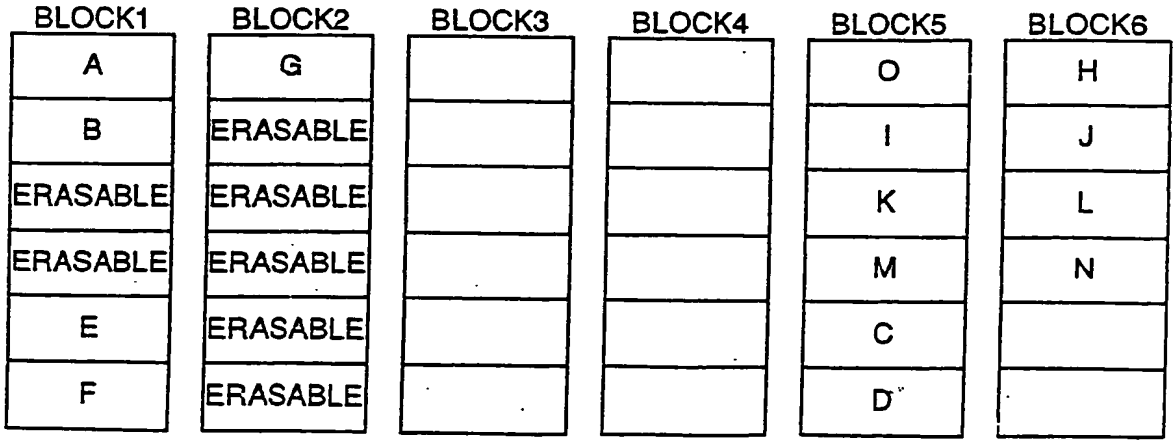


FIG.10G

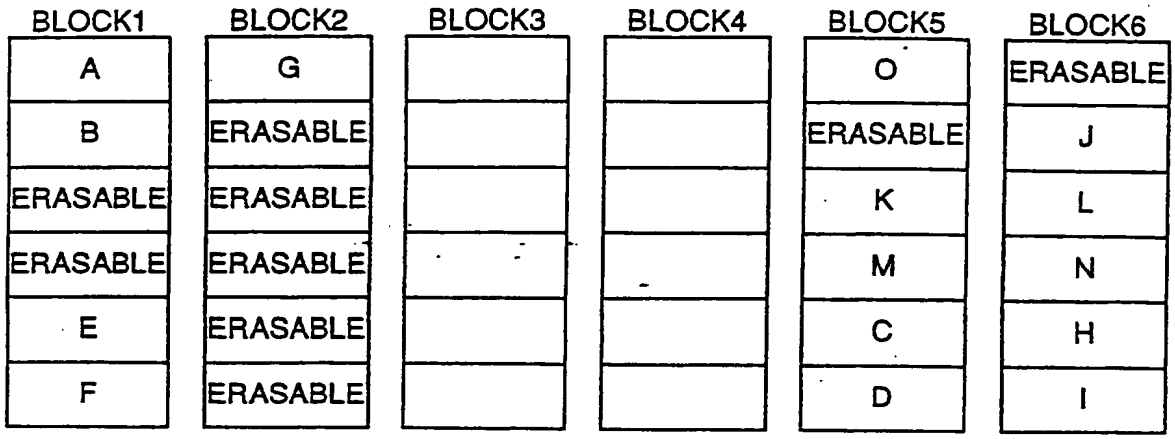


FIG.10H

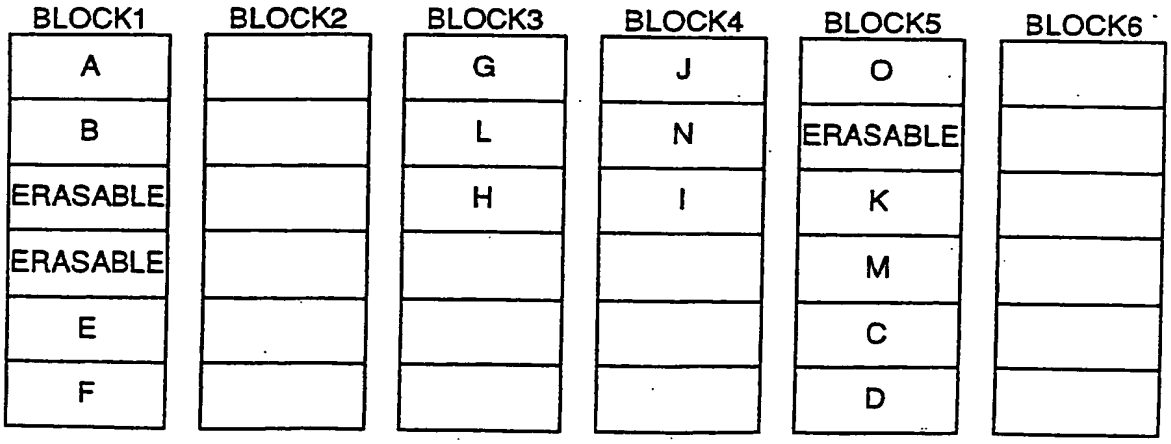


FIG.10I

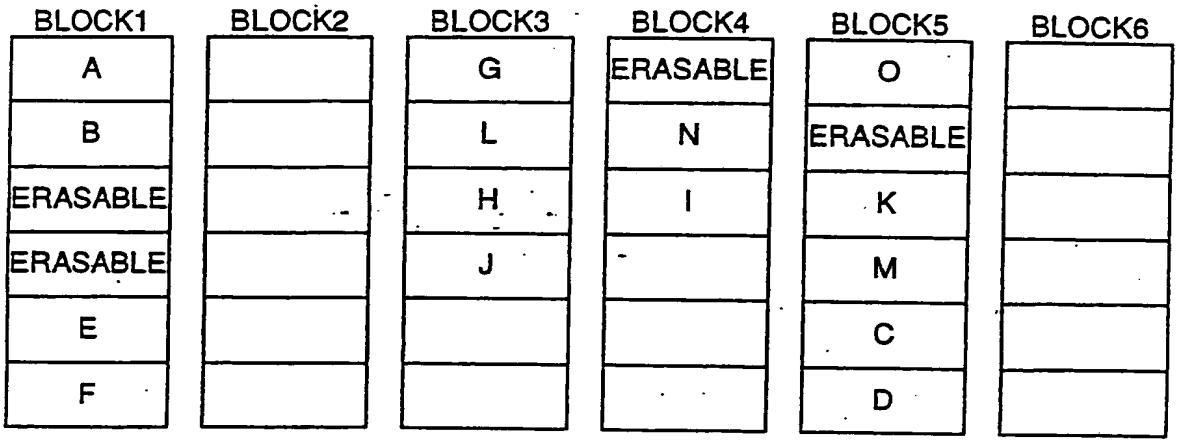


FIG.10J

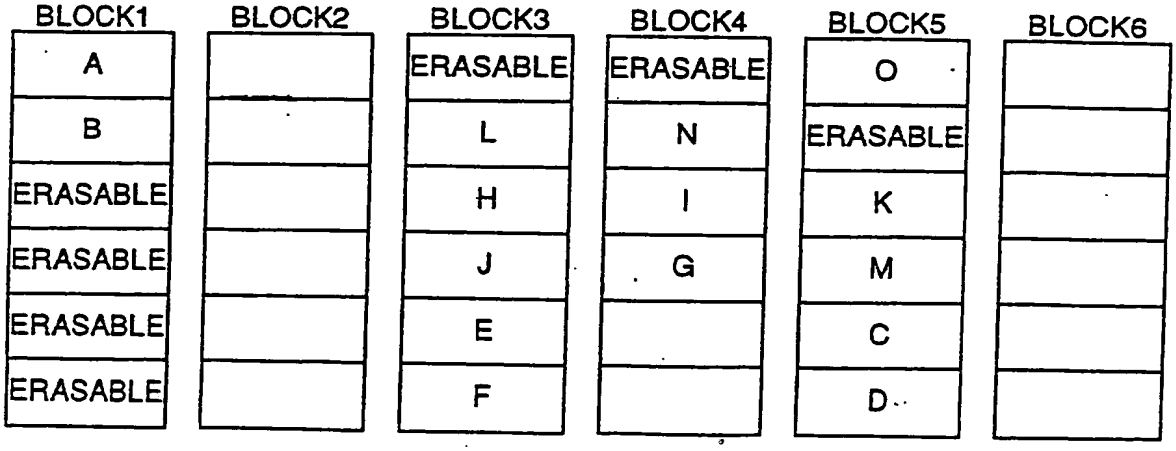


FIG.11

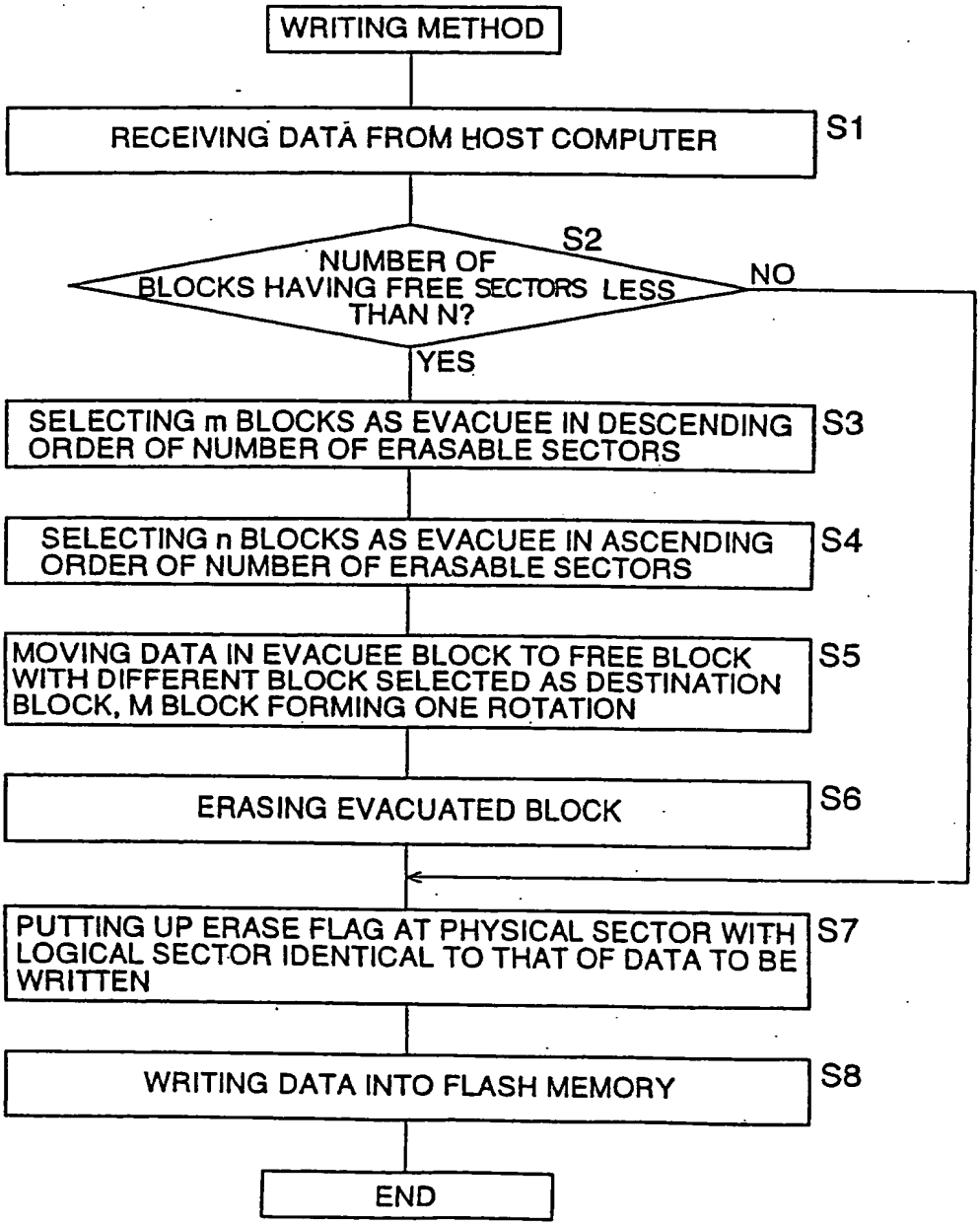

WRITING METHOD
RECEIVING DATA FROM HOST COMPUTER
S1
S2
NUMBER OF BLOCKS HAVING FREE SECTORS LESS THAN N?
NO
YES
SELECTING m BLOCKS AS EVACUEE IN DESCENDING ORDER OF NUMBER OF ERASABLE SECTORS
S3
SELECTING n BLOCKS AS EVACUEE IN ASCENDING ORDER OF NUMBER OF ERASABLE SECTORS
S4
MOVING DATA IN EVACUEE BLOCK TO FREE BLOCK WITH DIFFERENT BLOCK SELECTED AS DESTINATION BLOCK, M BLOCK FORMING ONE ROTATION
S5
ERASING EVACUATED BLOCK
S6
PUTTING UP ERASE FLAG AT PHYSICAL SECTOR WITH LOGICAL SECTOR IDENTICAL TO THAT OF DATA TO BE WRITTEN
S7
WRITING DATA INTO FLASH MEMORY
S8
END

FIG.12A

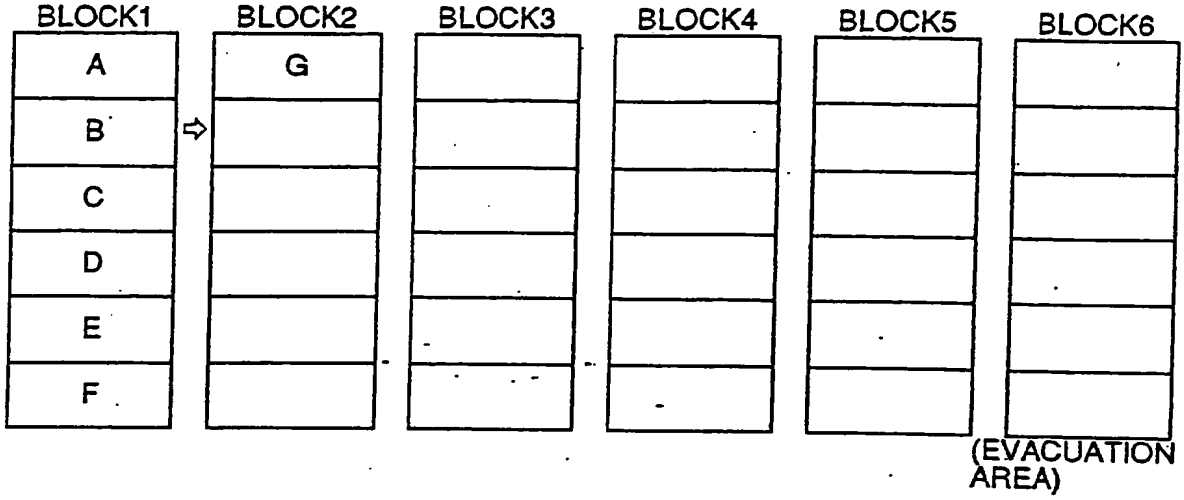


FIG.12B

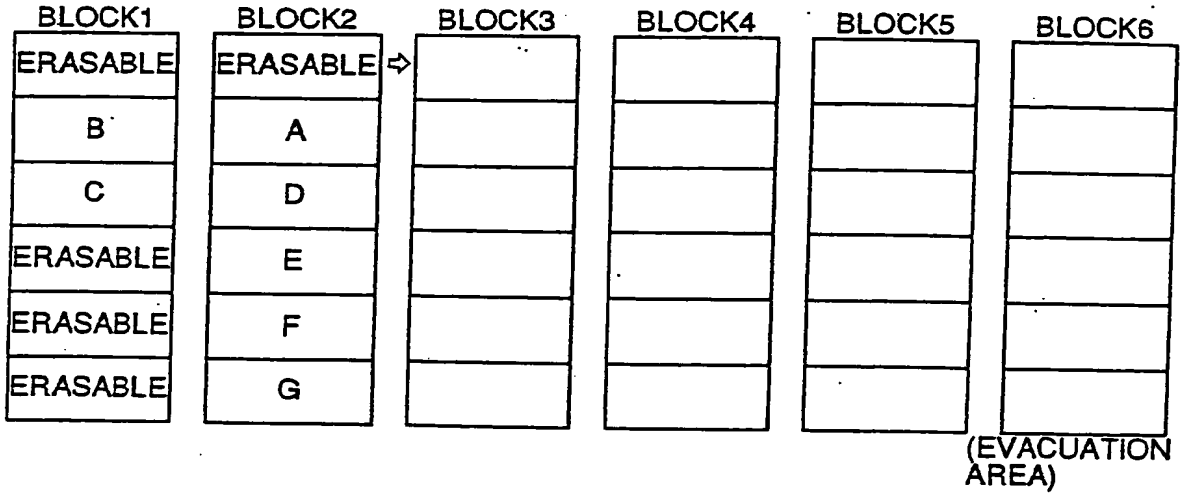


FIG.12C

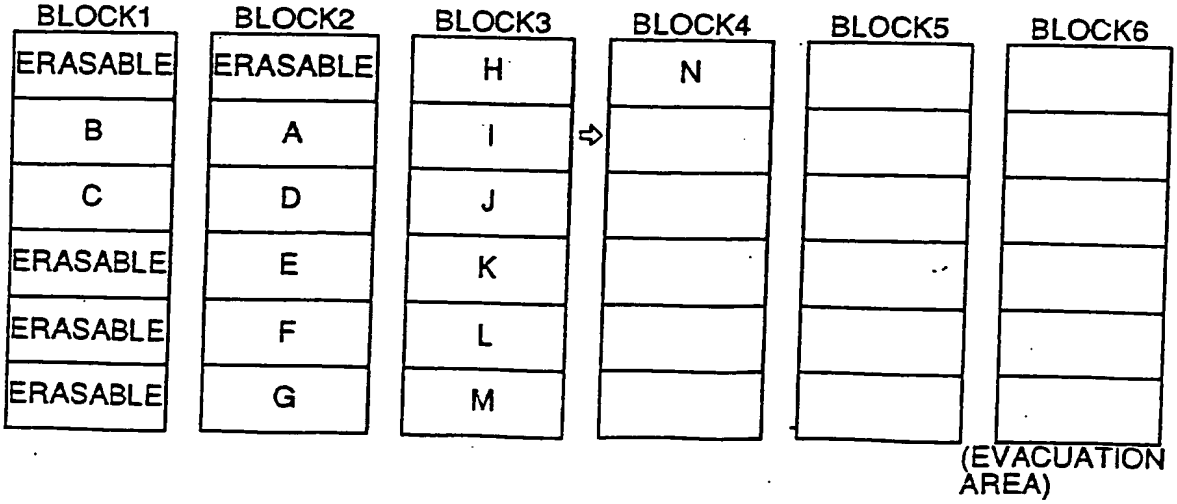


FIG.12D

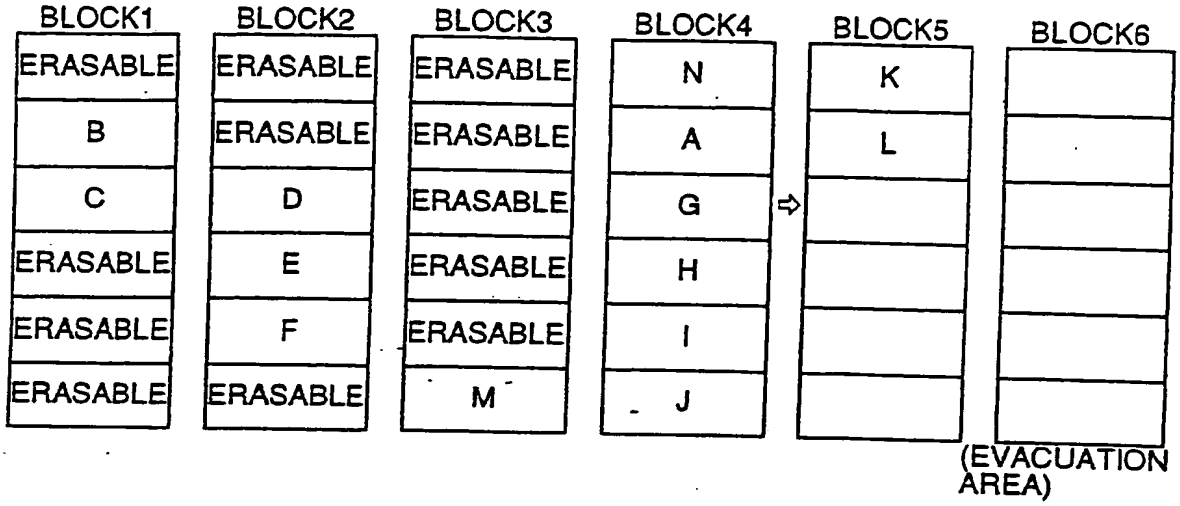


FIG.12E

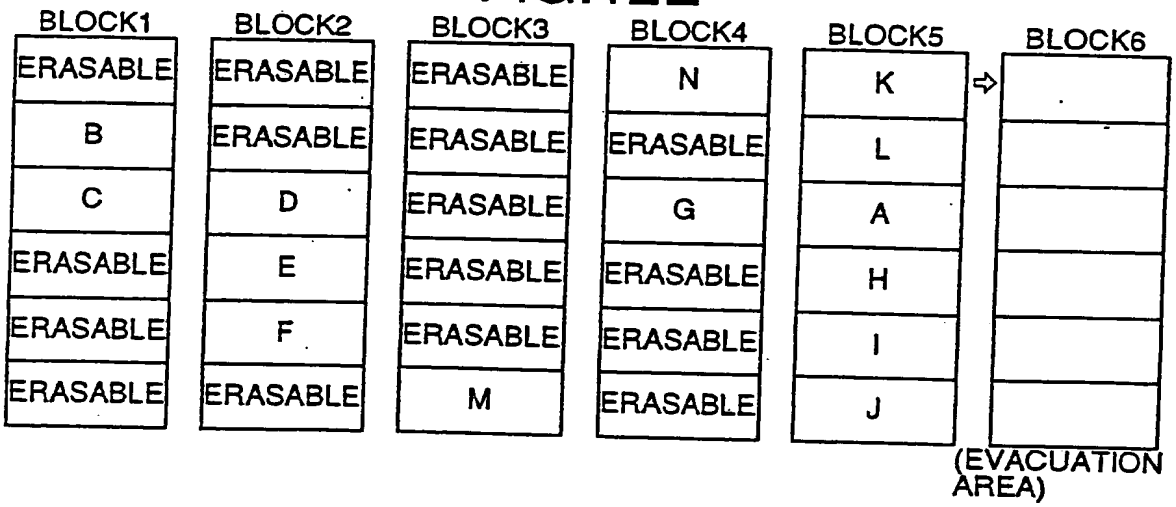


FIG.12F

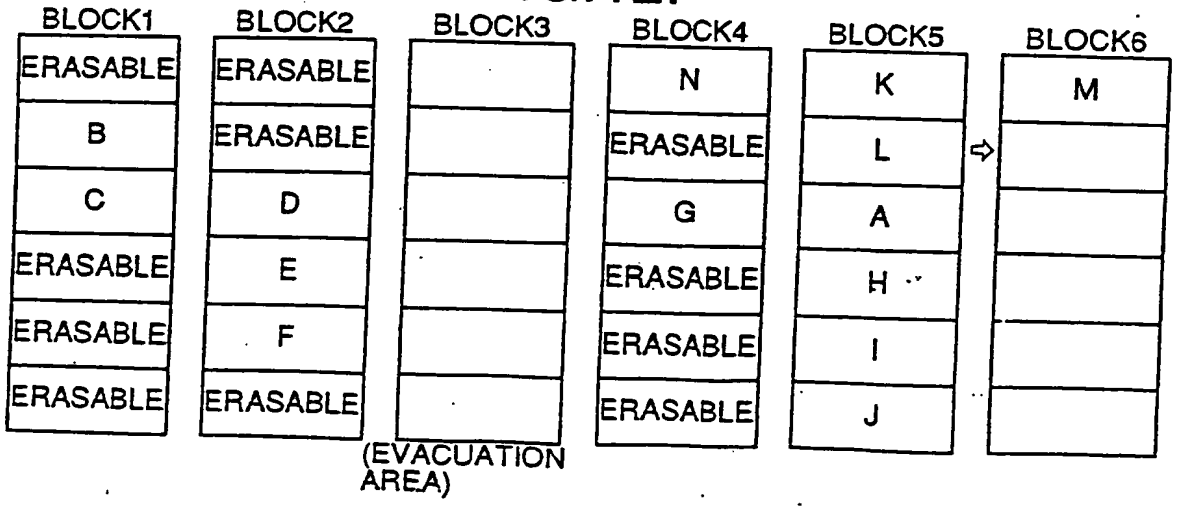


FIG.12G

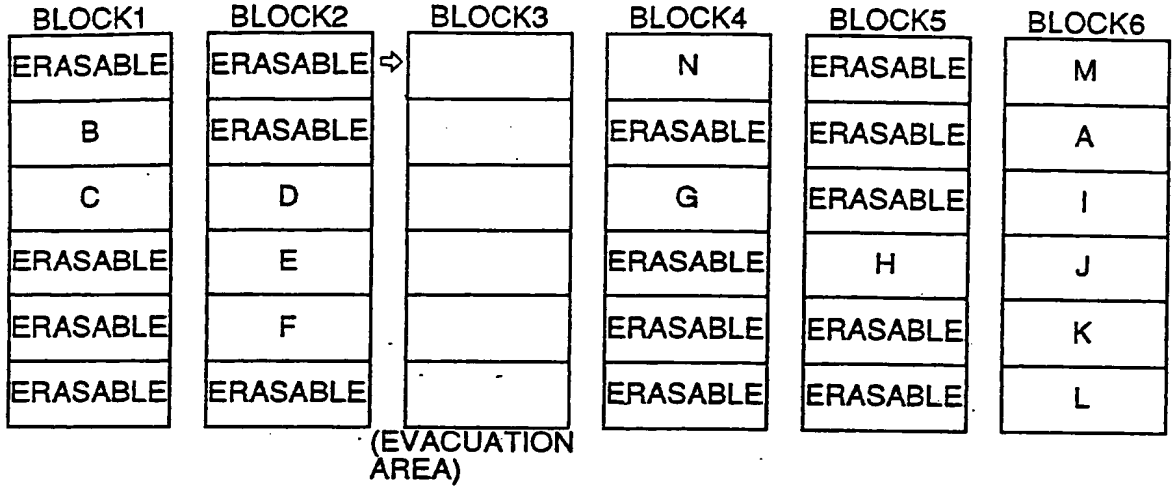


FIG.12H

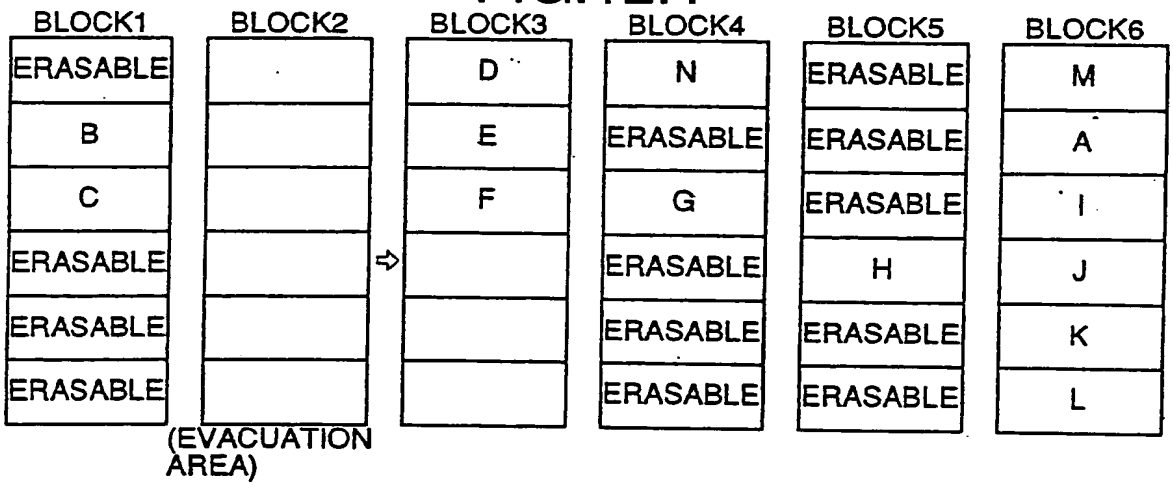


FIG.12I

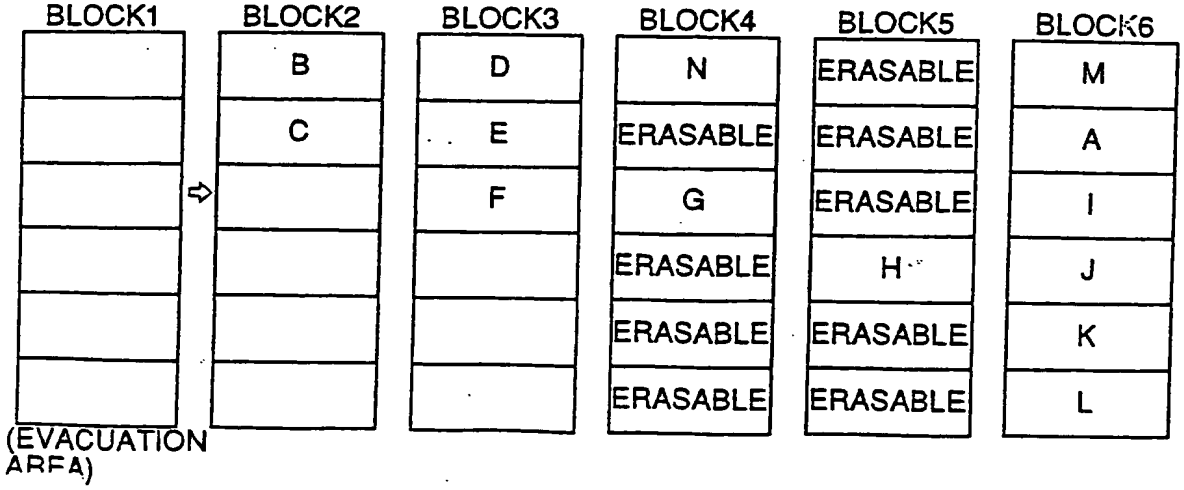


FIG.12J

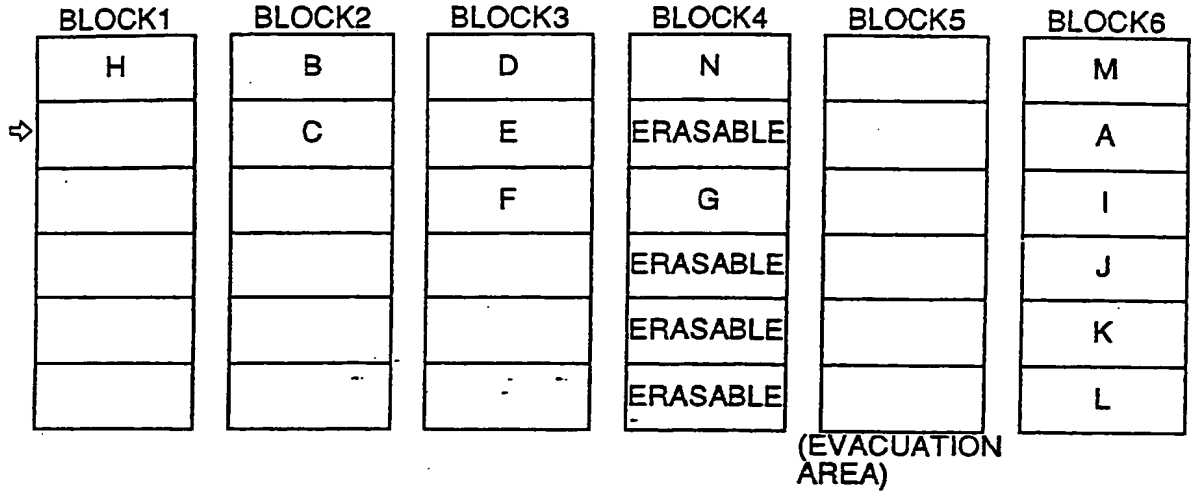


FIG.12K

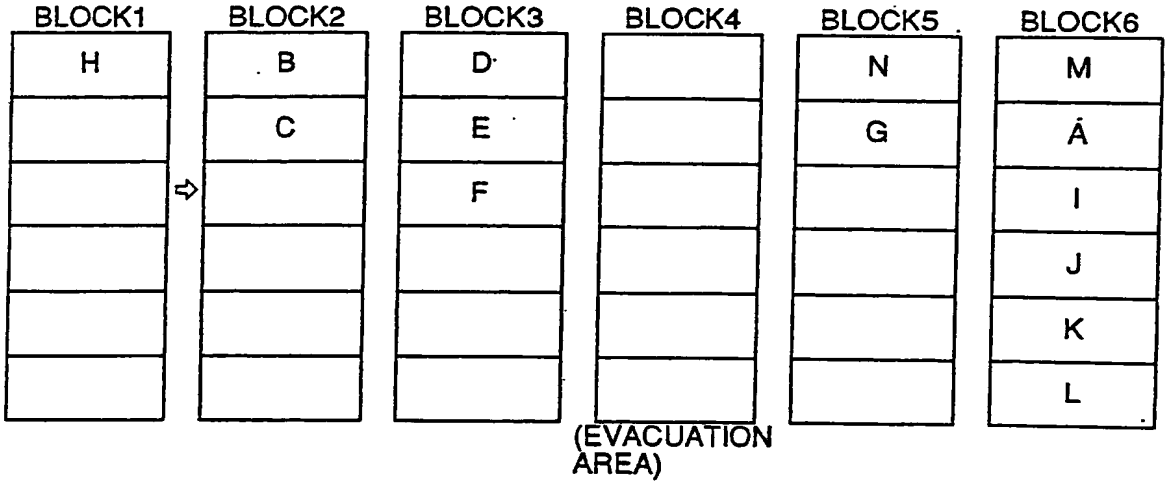


FIG.12L

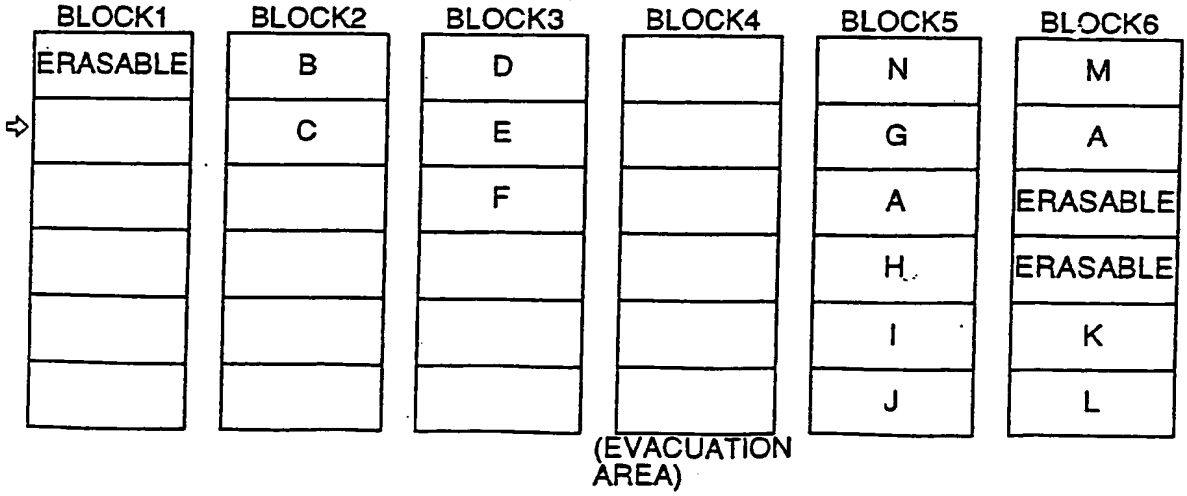


FIG.13

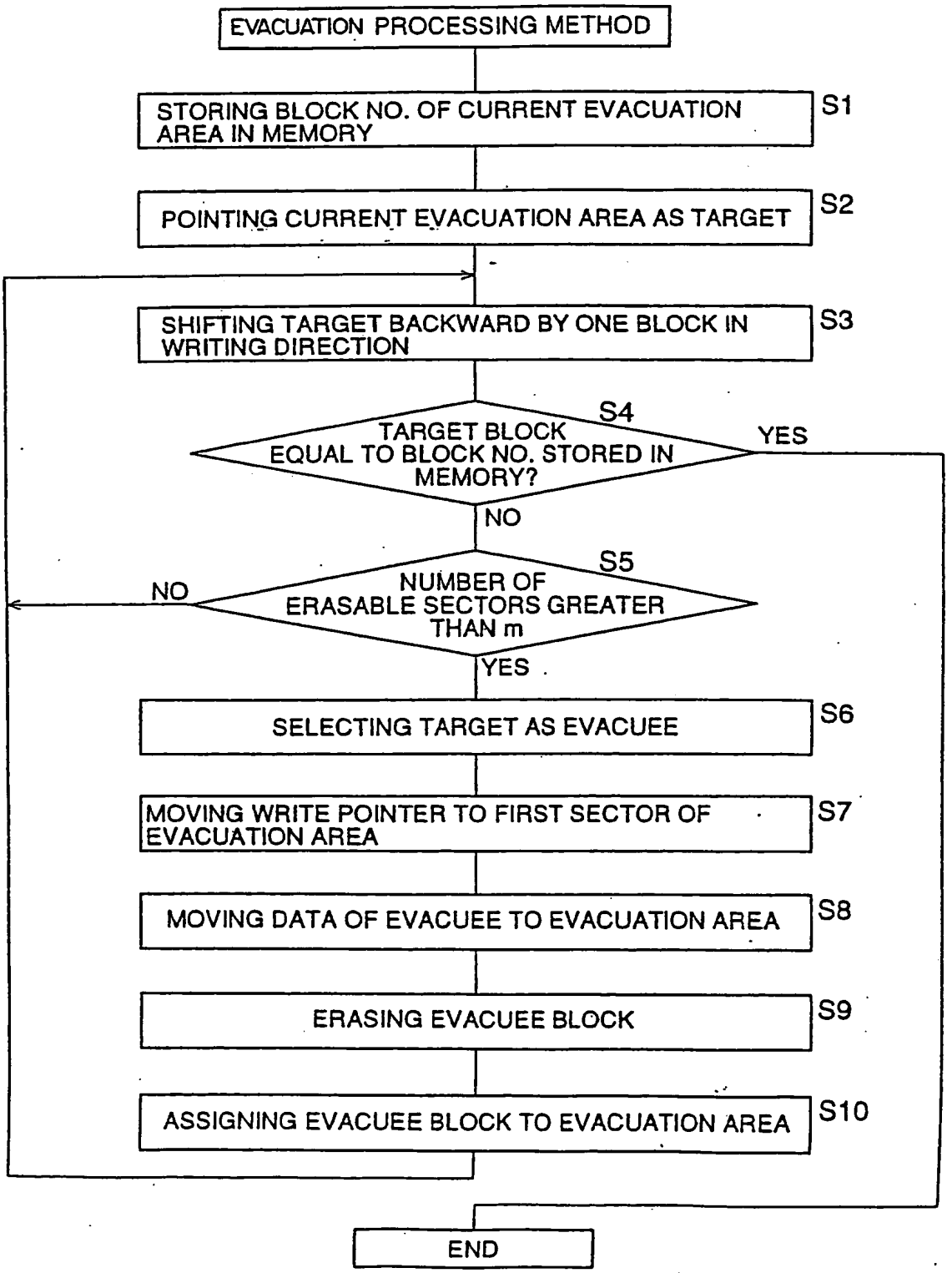

EVACUATION PROCESSING METHOD
STORING BLOCK NO. OF CURRENT EVACUATION AREA IN MEMORY
S1
POINTING CURRENT EVACUATION AREA AS TARGET
S2
SHIFTING TARGET BACKWARD BY ONE BLOCK IN WRITING DIRECTION
S3
S4
TARGET BLOCK EQUAL TO BLOCK NO. STORED IN MEMORY?
YES
NO
S5
NUMBER OF ERASABLE SECTORS GREATER THAN m
NO
YES
SELECTING TARGET AS EVACUEE
S6
MOVING WRITE POINTER TO FIRST SECTOR OF EVACUATION AREA
S7
MOVING DATA OF EVACUEE TO EVACUATION AREA
S8
ERASING EVACUEE BLOCK
S9
ASSIGNING EVACUEE BLOCK TO EVACUATION AREA
S10
END

FIG.14A

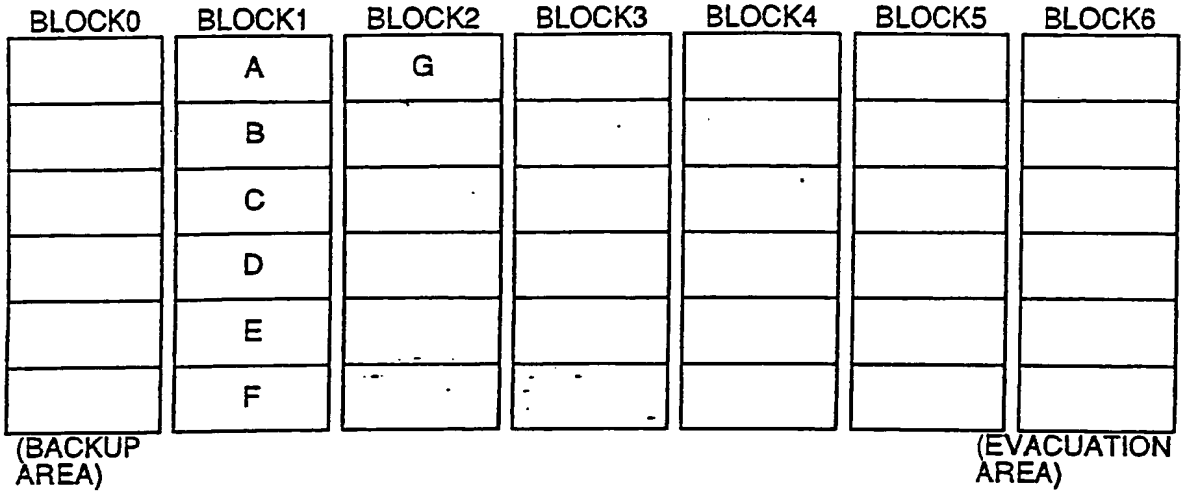


FIG.14B

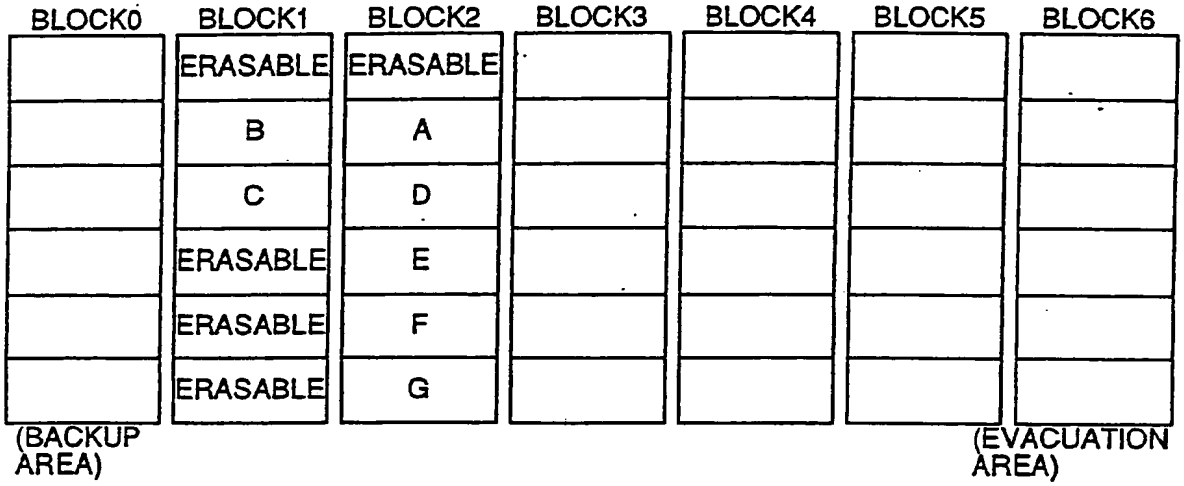


FIG.14C

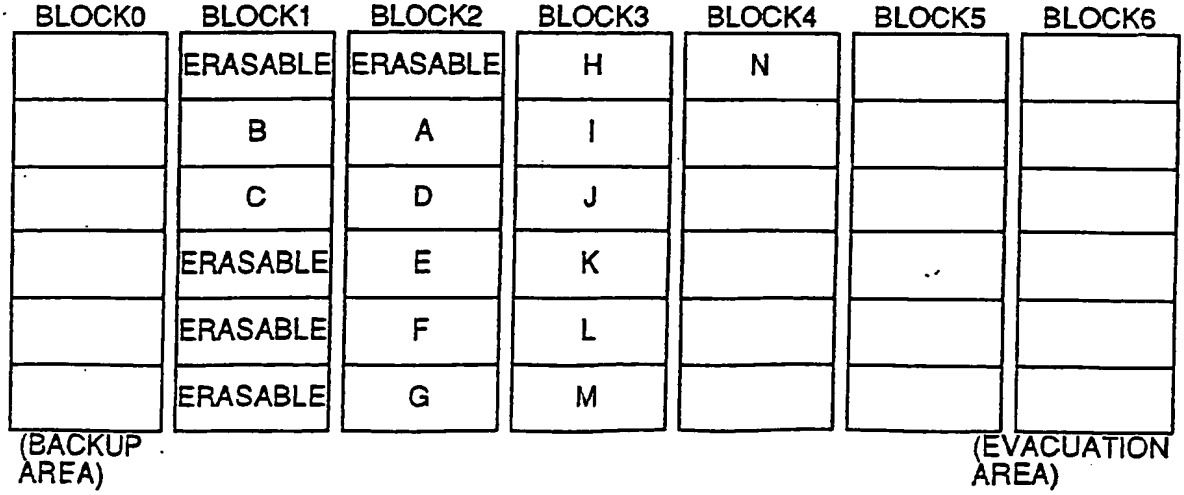


FIG.14D

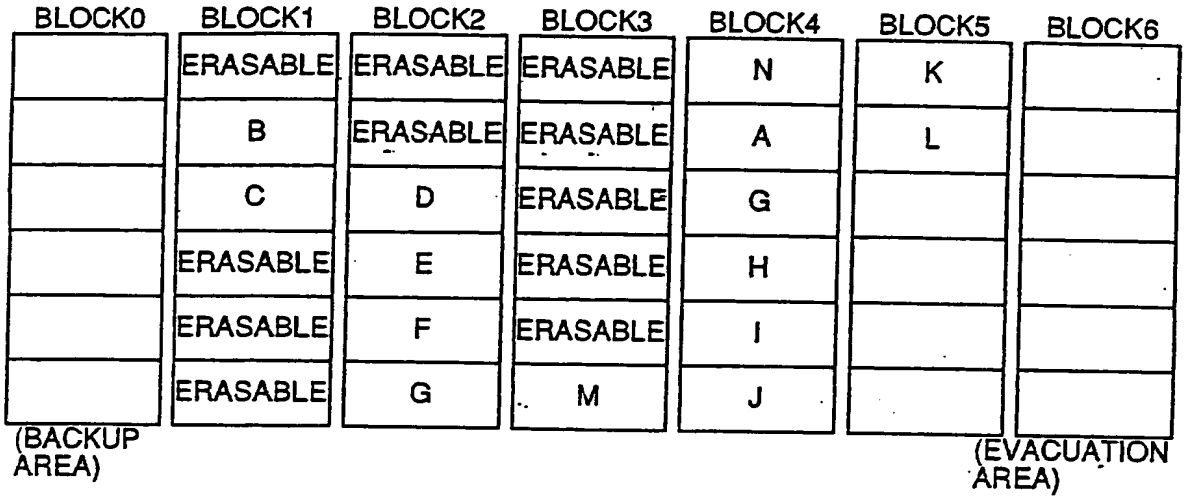


FIG.14E

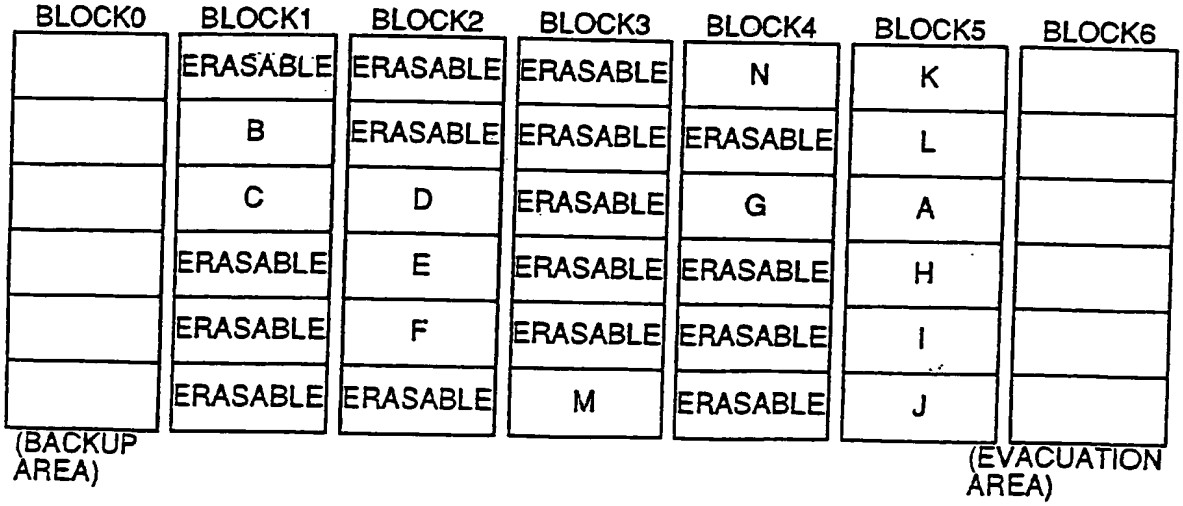


FIG.14F

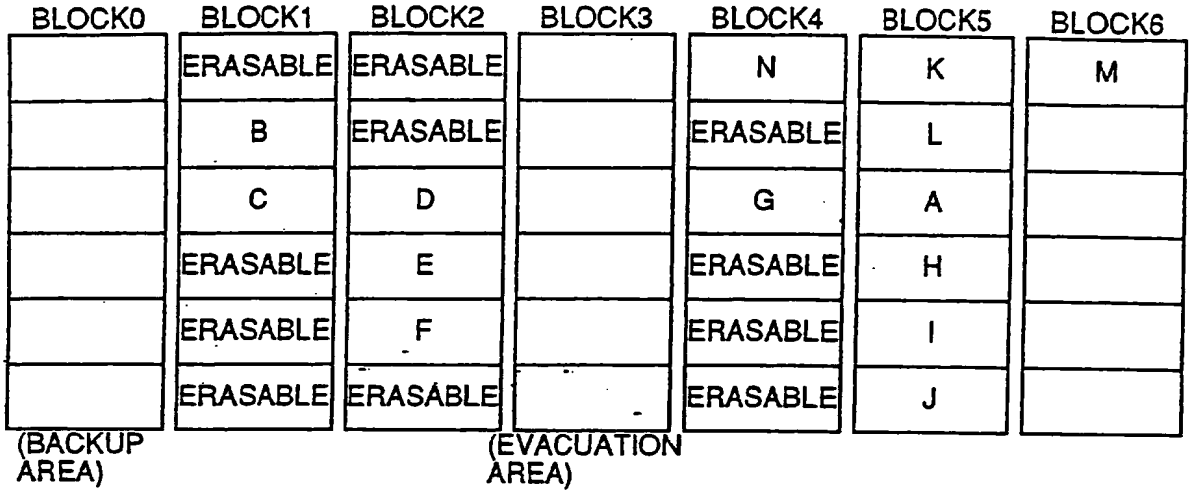


FIG.14G

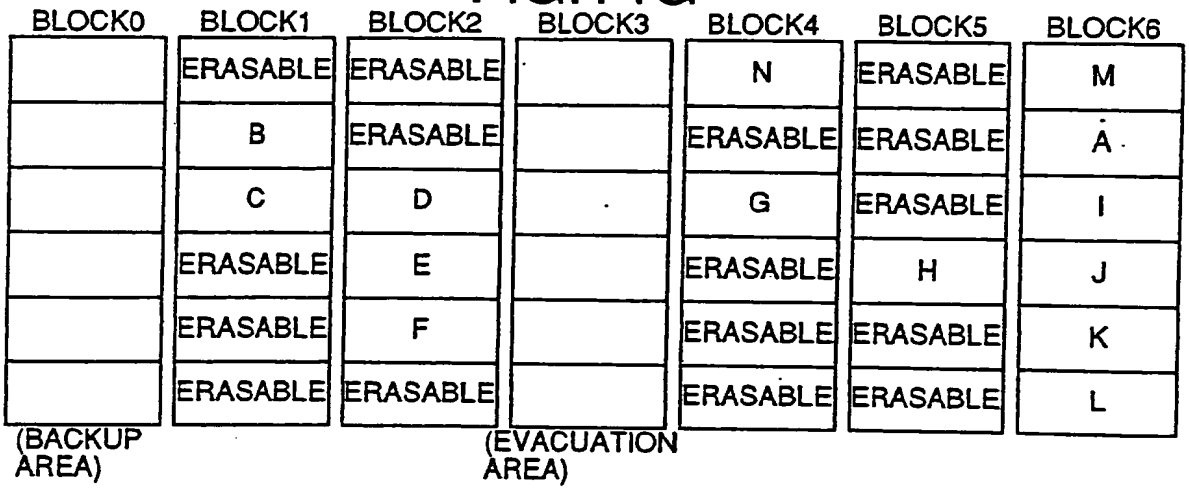


FIG.14H

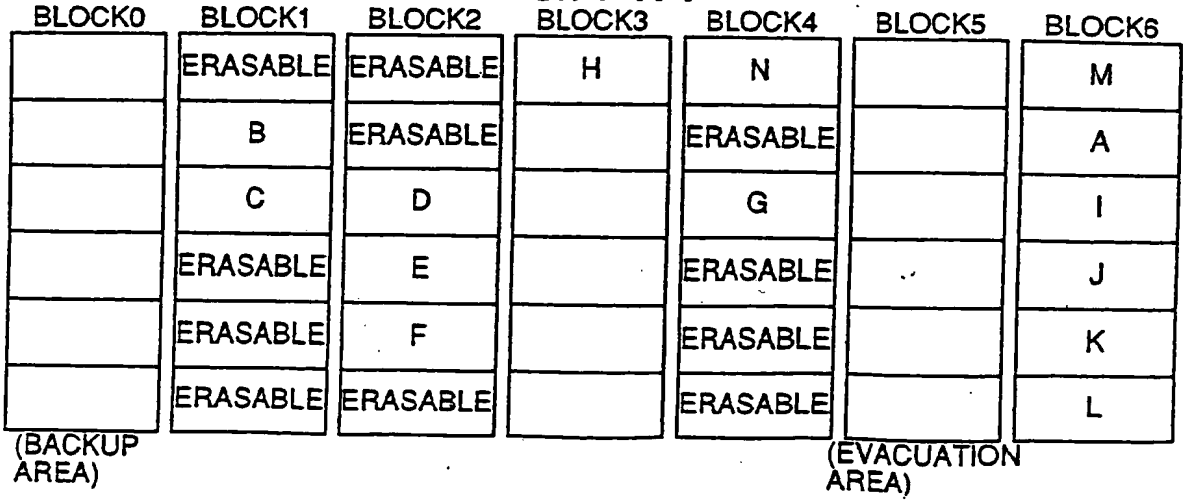


FIG.14I

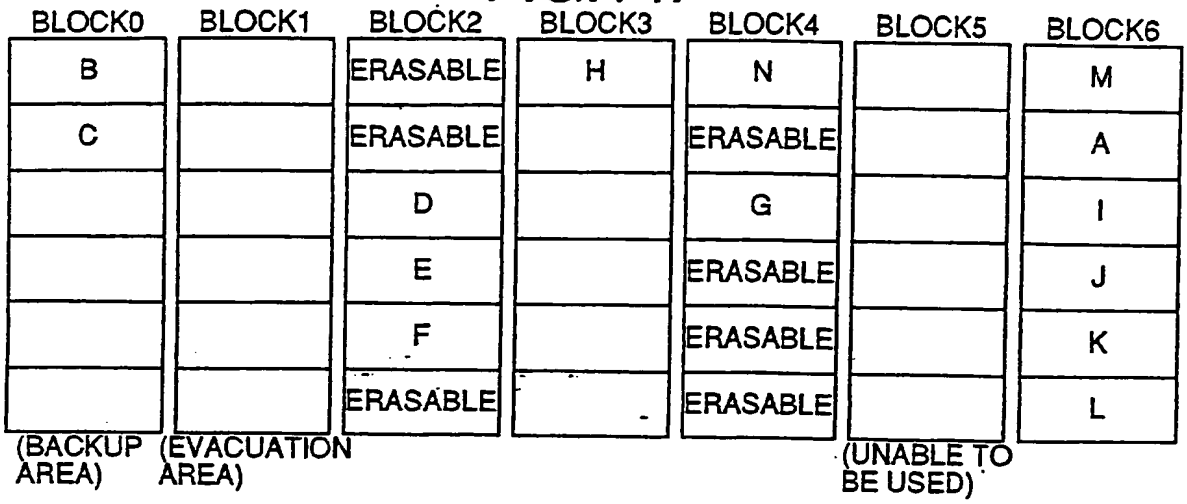


FIG.14J

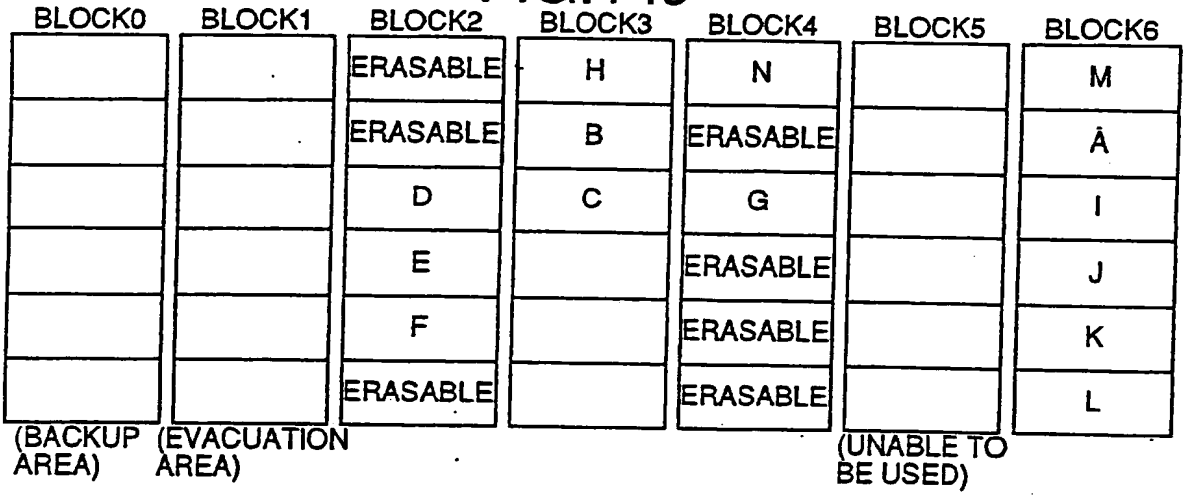


FIG.14K

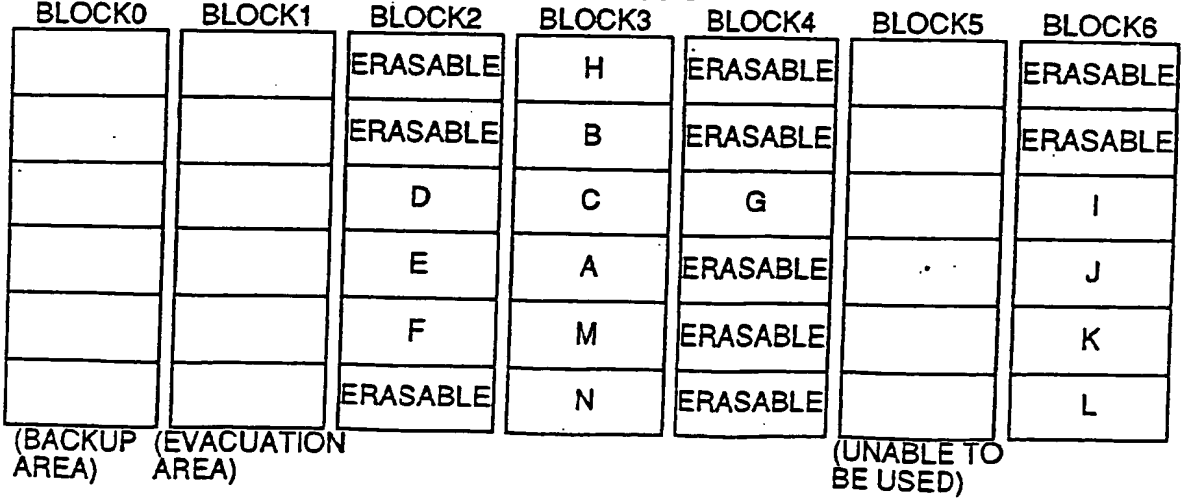


FIG.14L

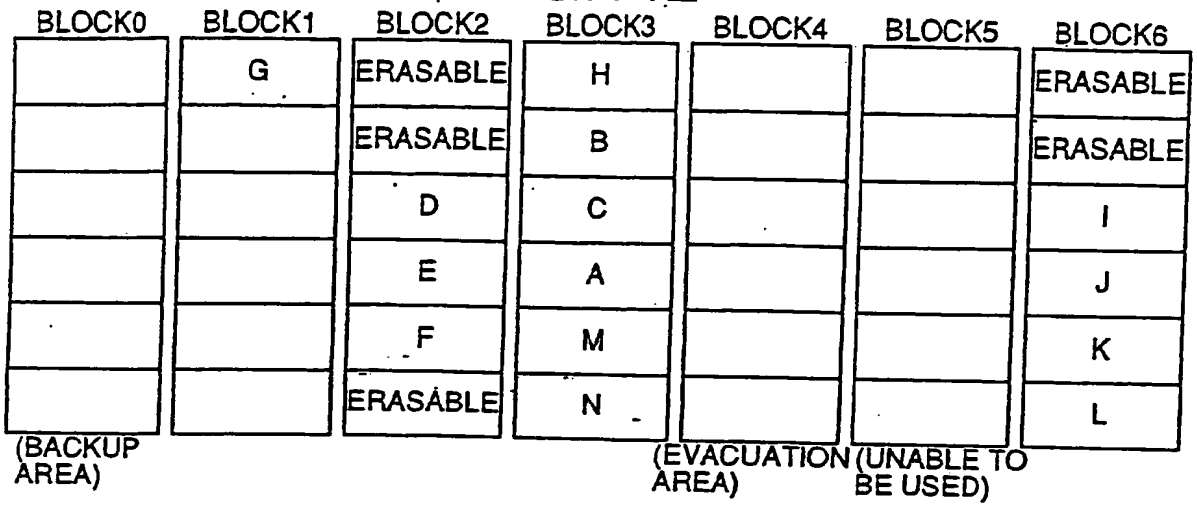


FIG.14M

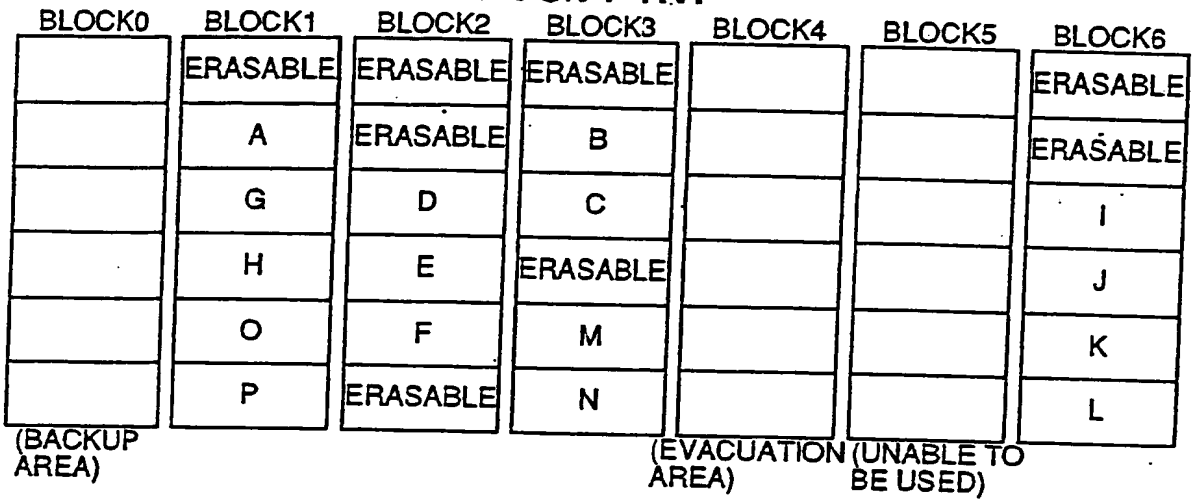


FIG.14N

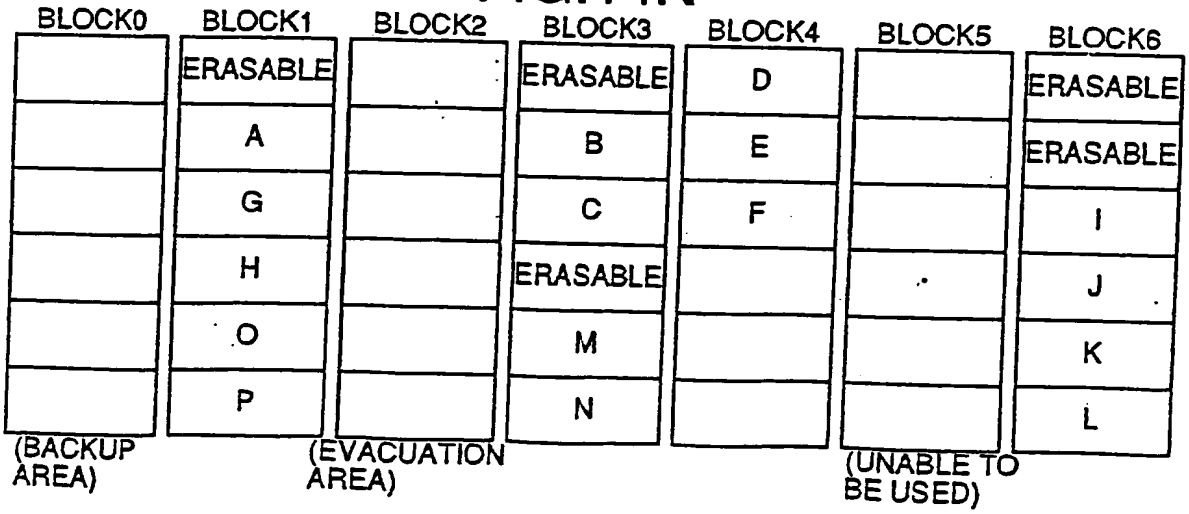


FIG.14O

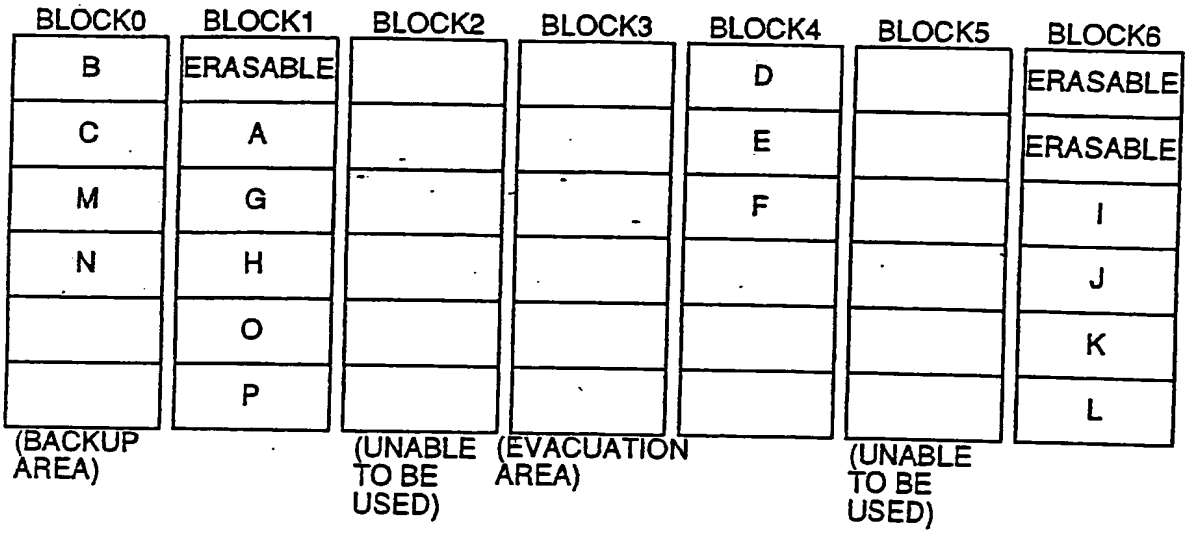


FIG.14P

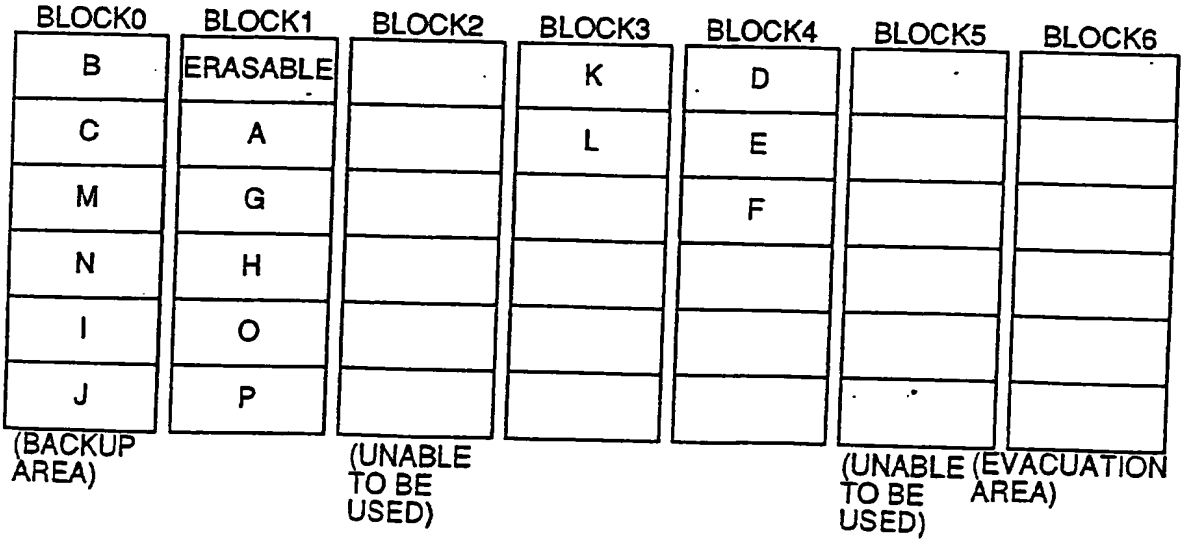


FIG.14Q

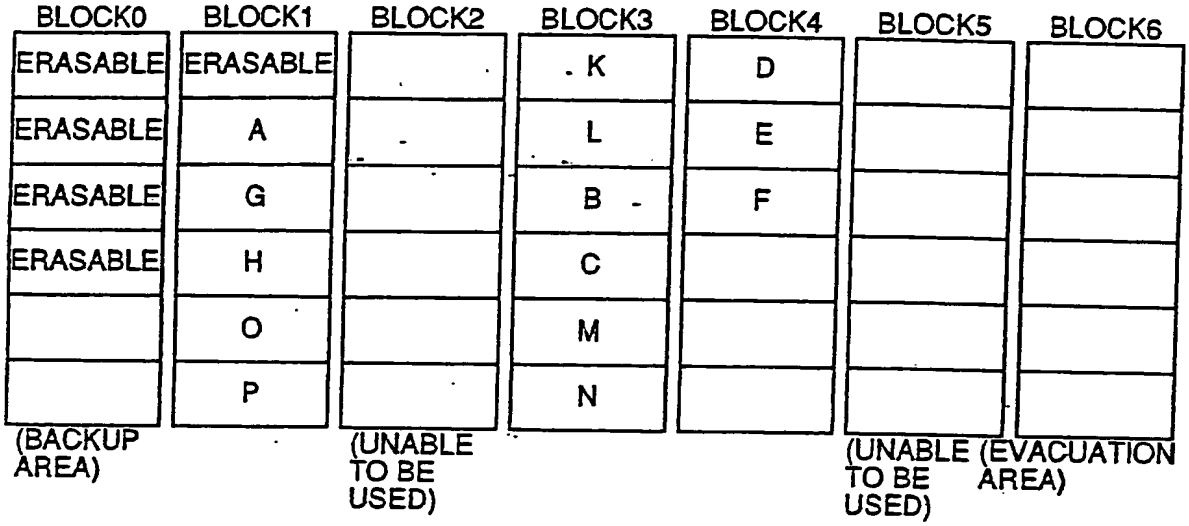


FIG.14R

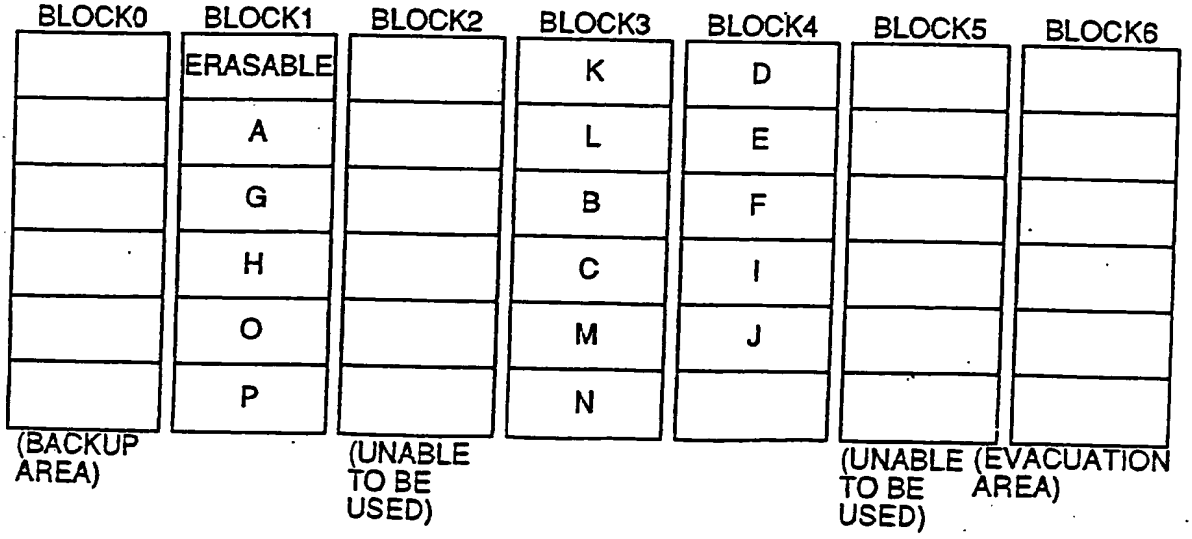


FIG.15

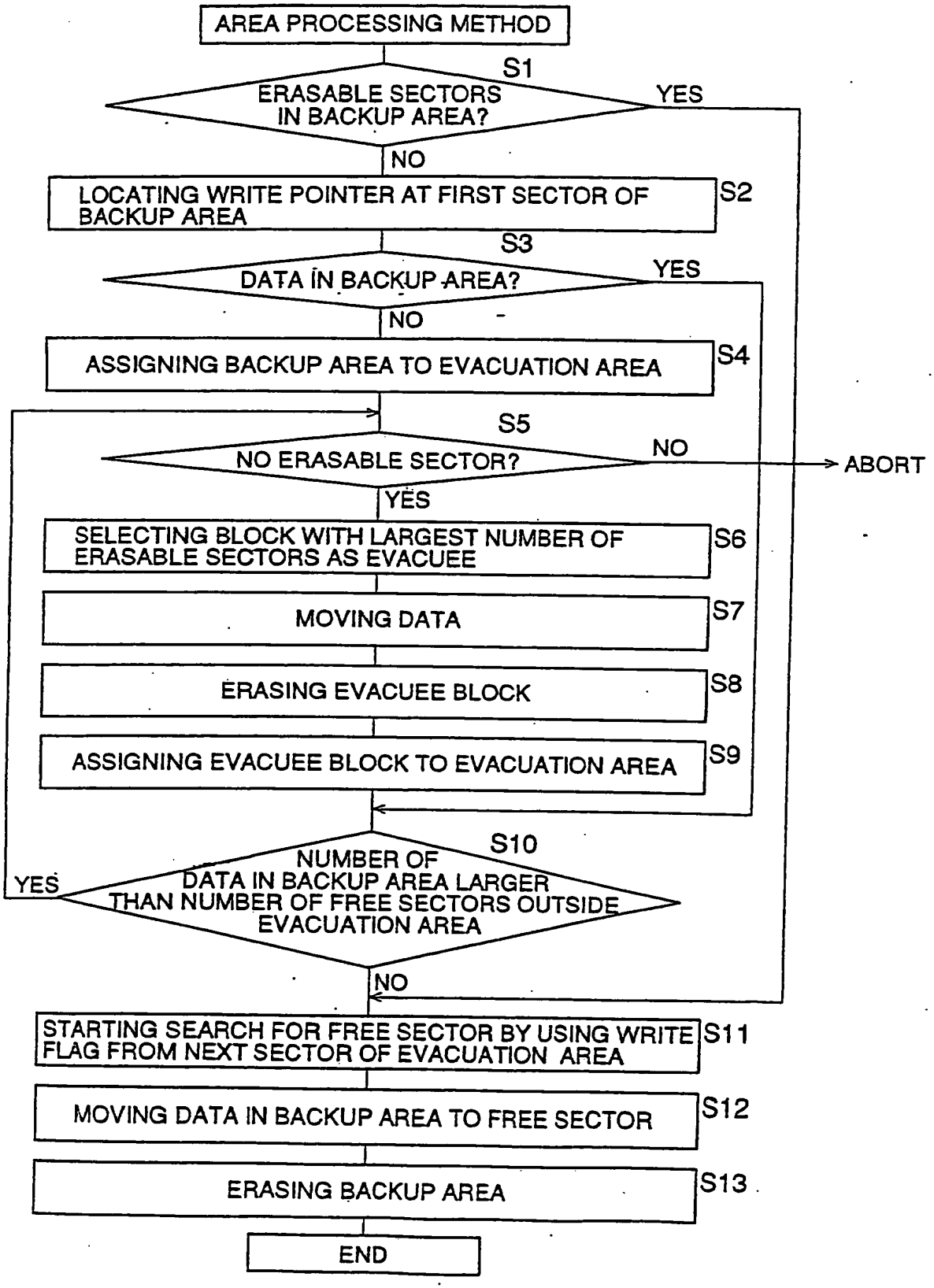

AREA PROCESSING METHOD
S1
ERASABLE SECTORS IN BACKUP AREA?
YES
NO
LOCATING WRITE POINTER AT FIRST SECTOR OF BACKUP AREA
S2
S3
DATA IN BACKUP AREA?
YES
NO
ASSIGNING BACKUP AREA TO EVACUATION AREA
S4
S5
NO ERASABLE SECTOR?
NO
ABORT
YES
SELECTING BLOCK WITH LARGEST NUMBER OF ERASABLE SECTORS AS EVACUEE
S6
MOVING DATA
S7
ERASING EVACUEE BLOCK
S8
ASSIGNING EVACUEE BLOCK TO EVACUATION AREA
S9
S10
NUMBER OF DATA IN BACKUP AREA LARGER THAN NUMBER OF FREE SECTORS OUTSIDE EVACUATION AREA
YES
NO
STARTING SEARCH FOR FREE SECTOR BY USING WRITE FLAG FROM NEXT SECTOR OF EVACUATION AREA
S11
MOVING DATA IN BACKUP AREA TO FREE SECTOR
S12
ERASING BACKUP AREA
S13
END

FIG.16A

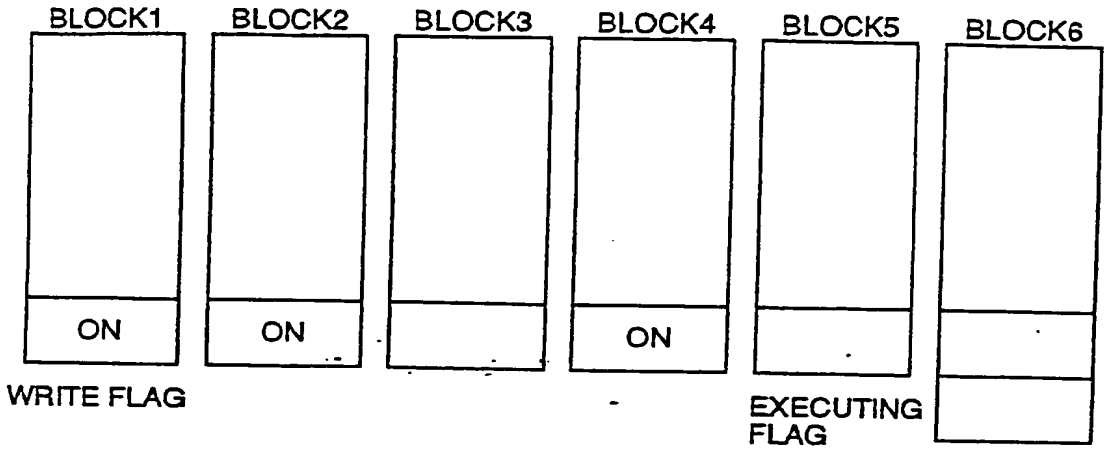


FIG.16B

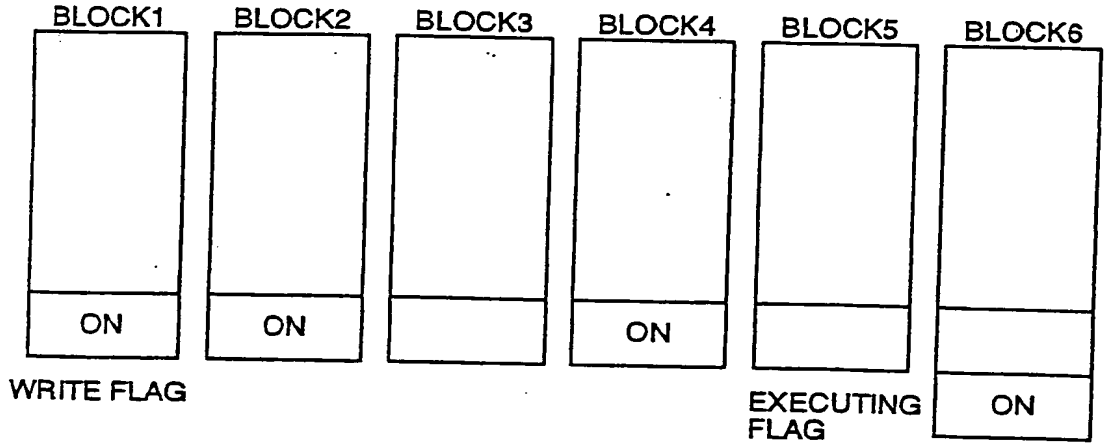


FIG.16C

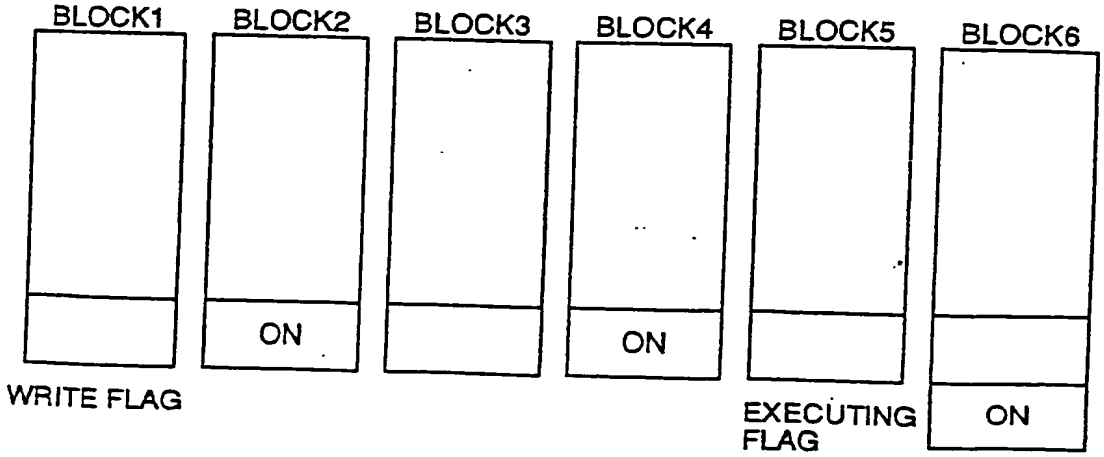


FIG.16D

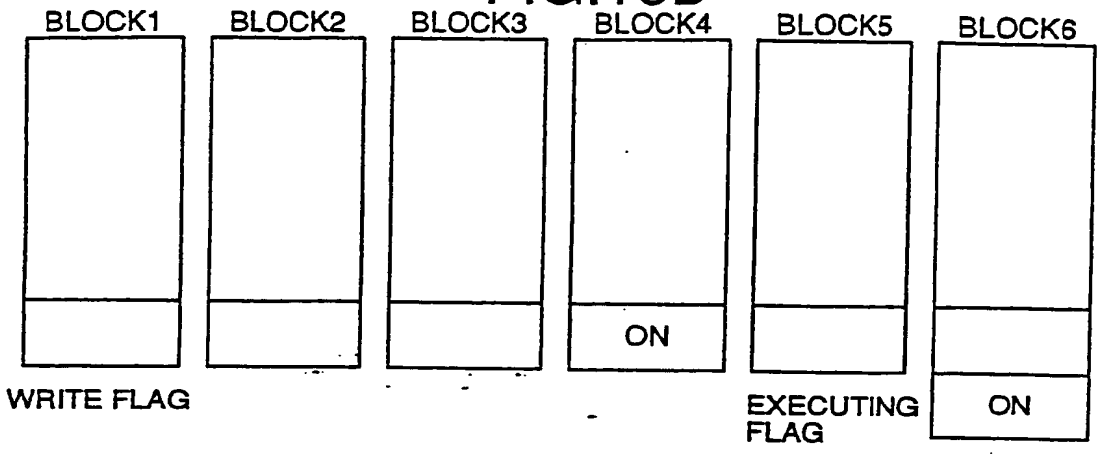


FIG.16E

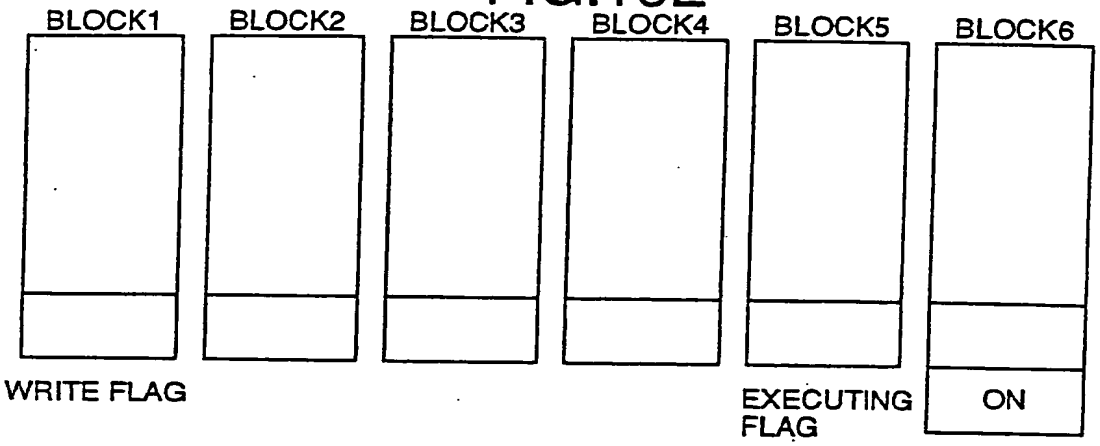


FIG.16F

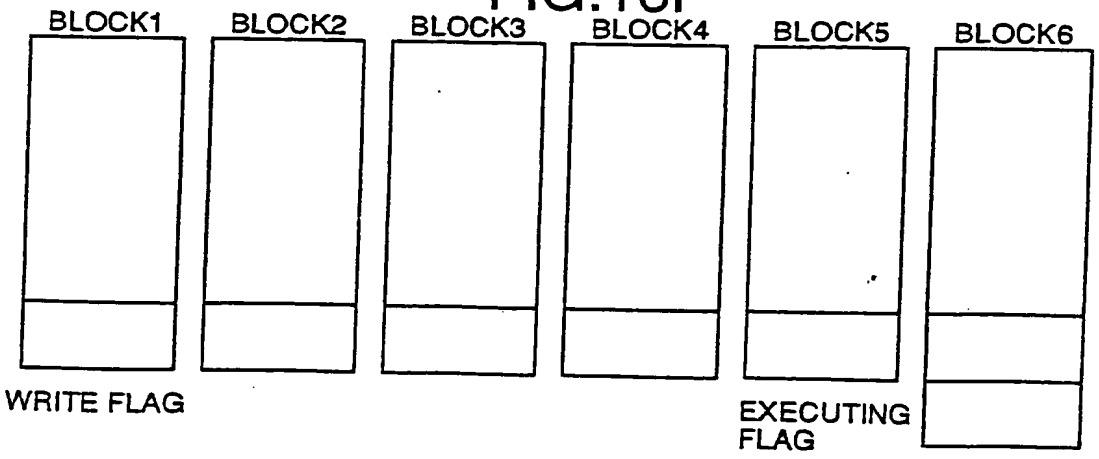


FIG.17

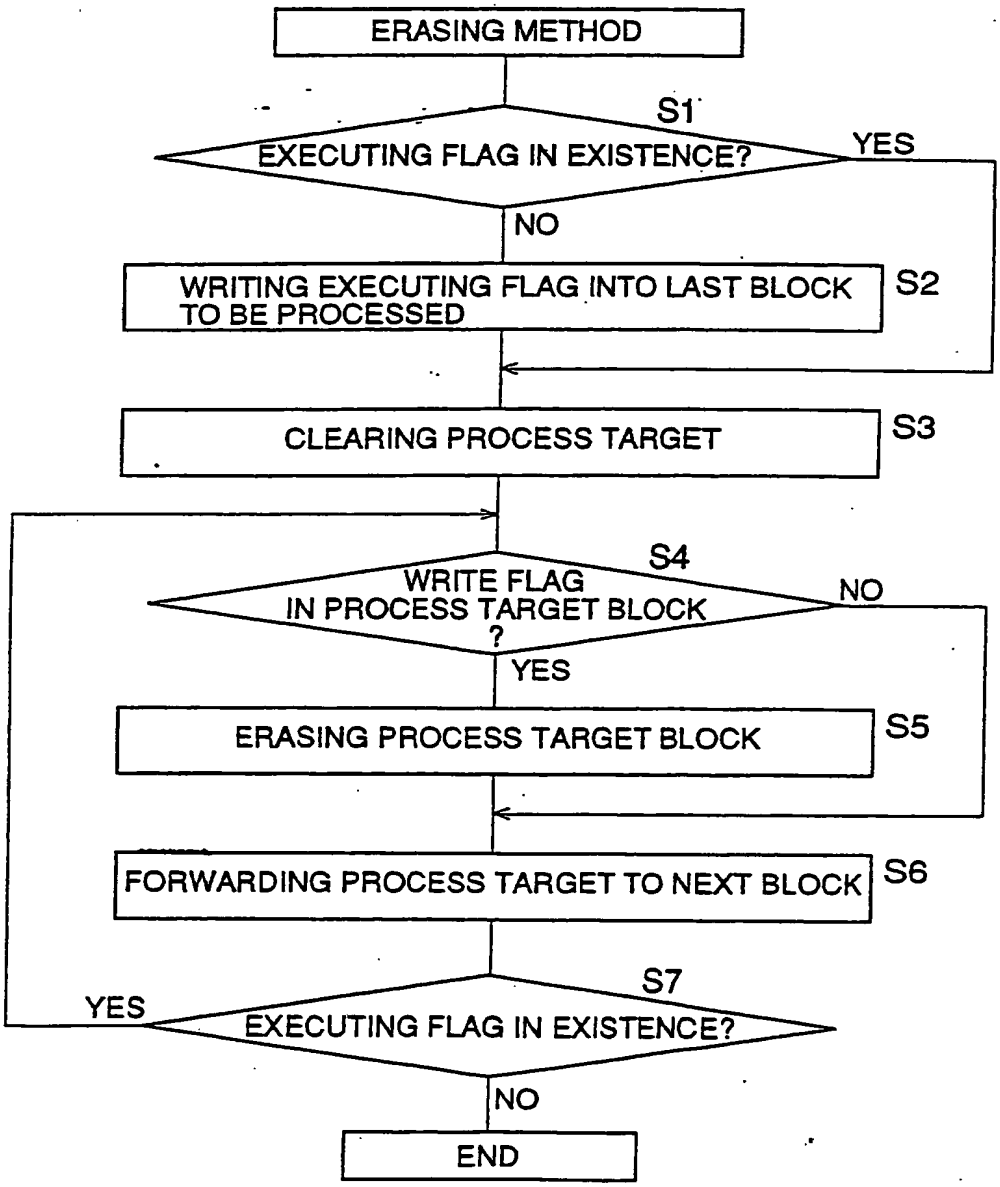

ERASING METHOD
S1
EXECUTING FLAG IN EXISTENCE?
YES
NO
WRITING EXECUTING FLAG INTO LAST BLOCK TO BE PROCESSED
S2
CLEARING PROCESS TARGET
S3
S4
WRITE FLAG IN PROCESS TARGET BLOCK ?
NO
YES
ERASING PROCESS TARGET BLOCK
S5
FORWARDING PROCESS TARGET TO NEXT BLOCK
S6
S7
YES
EXECUTING FLAG IN EXISTENCE?
NO
END

FIG.18

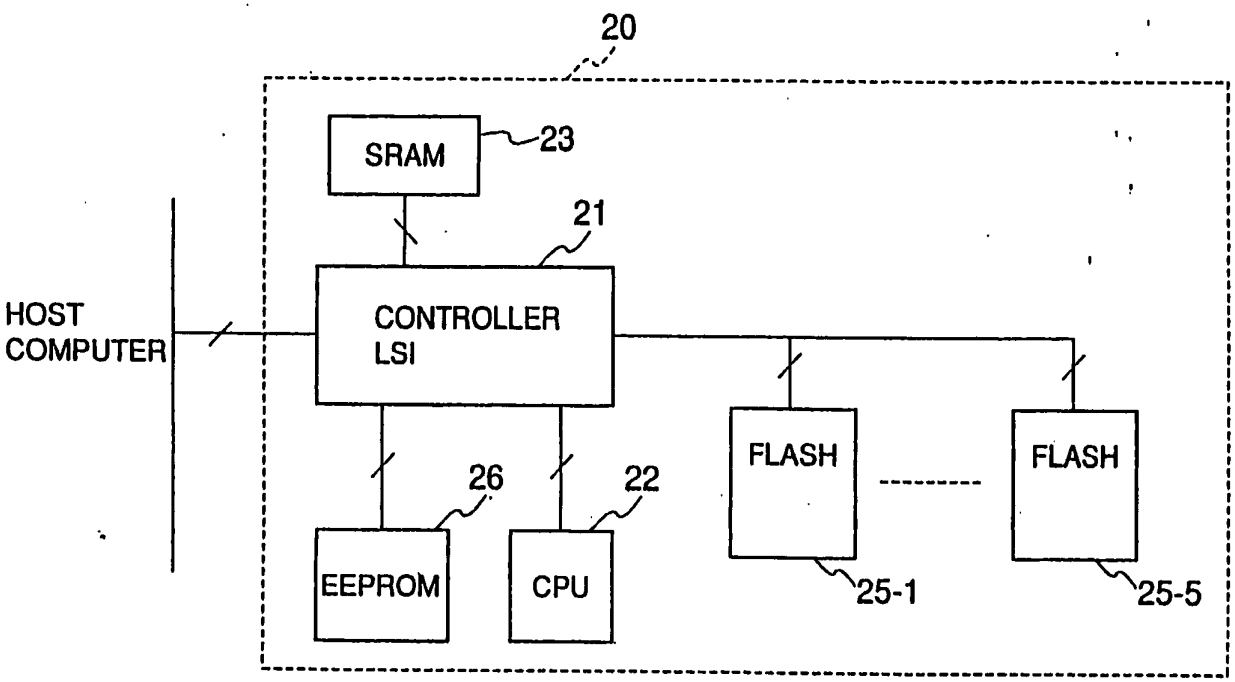

20
SRAM
23
21
HOST
COMPUTER
CONTROLLER
LSI
FLASH
FLASH
26
22
EEPROM
CPU
25-1
25-5

FIG.19A

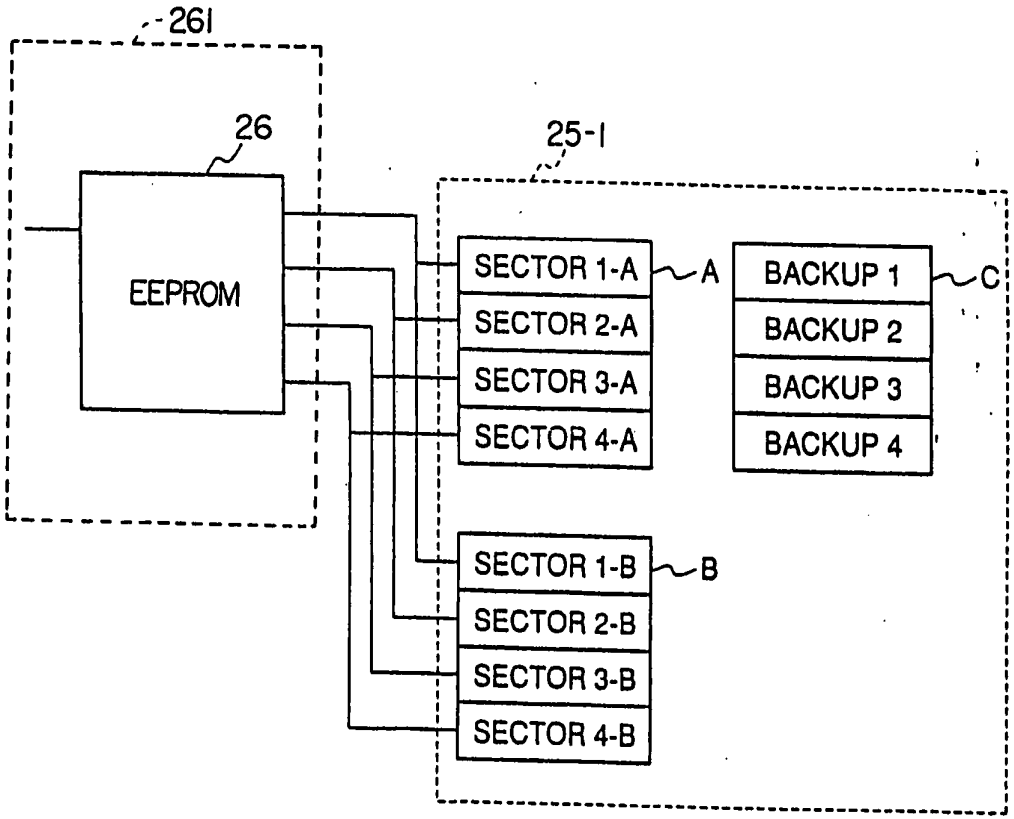

261
26
25-1
EEPROM
SECTOR 1-A
SECTOR 2-A
SECTOR 3-A
SECTOR 4-A
A
BACKUP 1
BACKUP 2
BACKUP 3
BACKUP 4
C
SECTOR 1-B
SECTOR 2-B
SECTOR 3-B
SECTOR 4-B
B

FIG.19B

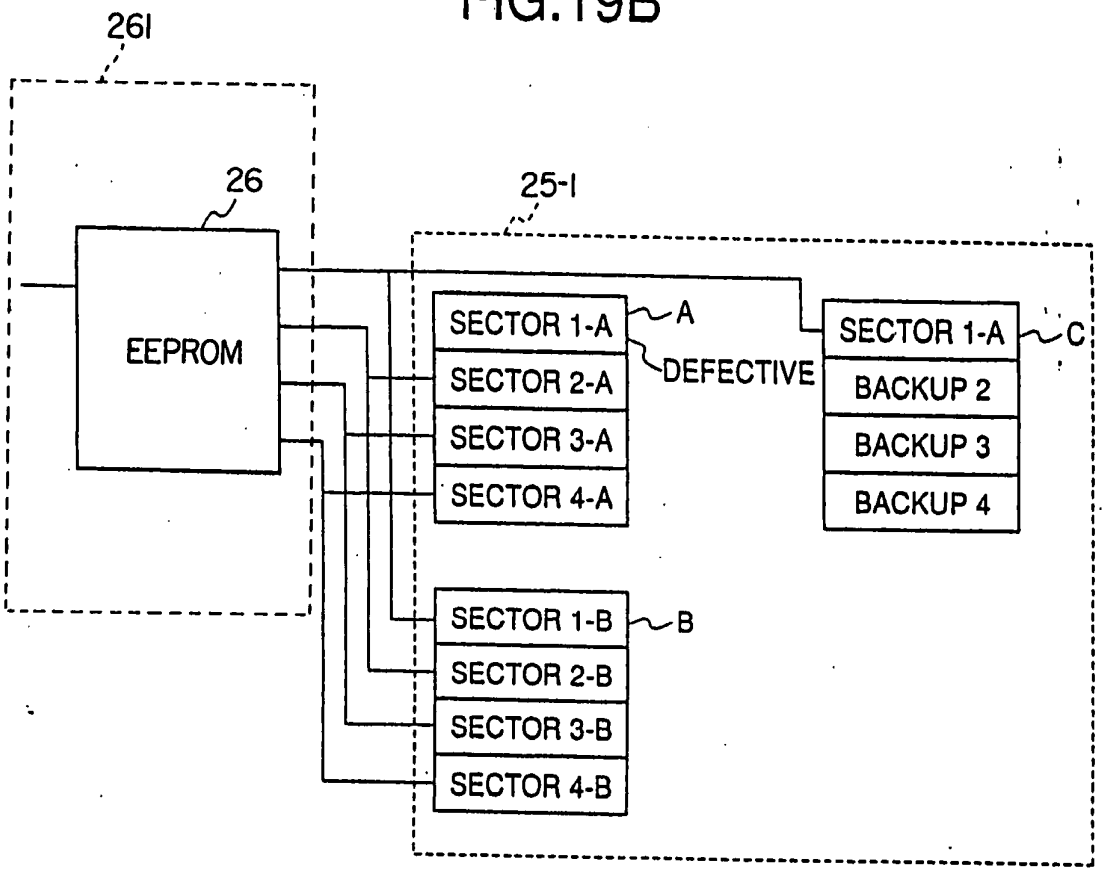

261
26
25-I
EEPROM
SECTOR 1-A
A
DEFECTIVE
SECTOR 2-A
SECTOR 3-A
SECTOR 4-A
SECTOR 1-A
C
BACKUP 2
BACKUP 3
BACKUP 4
SECTOR 1-B
B
SECTOR 2-B
SECTOR 3-B
SECTOR 4-B

FIG.20A

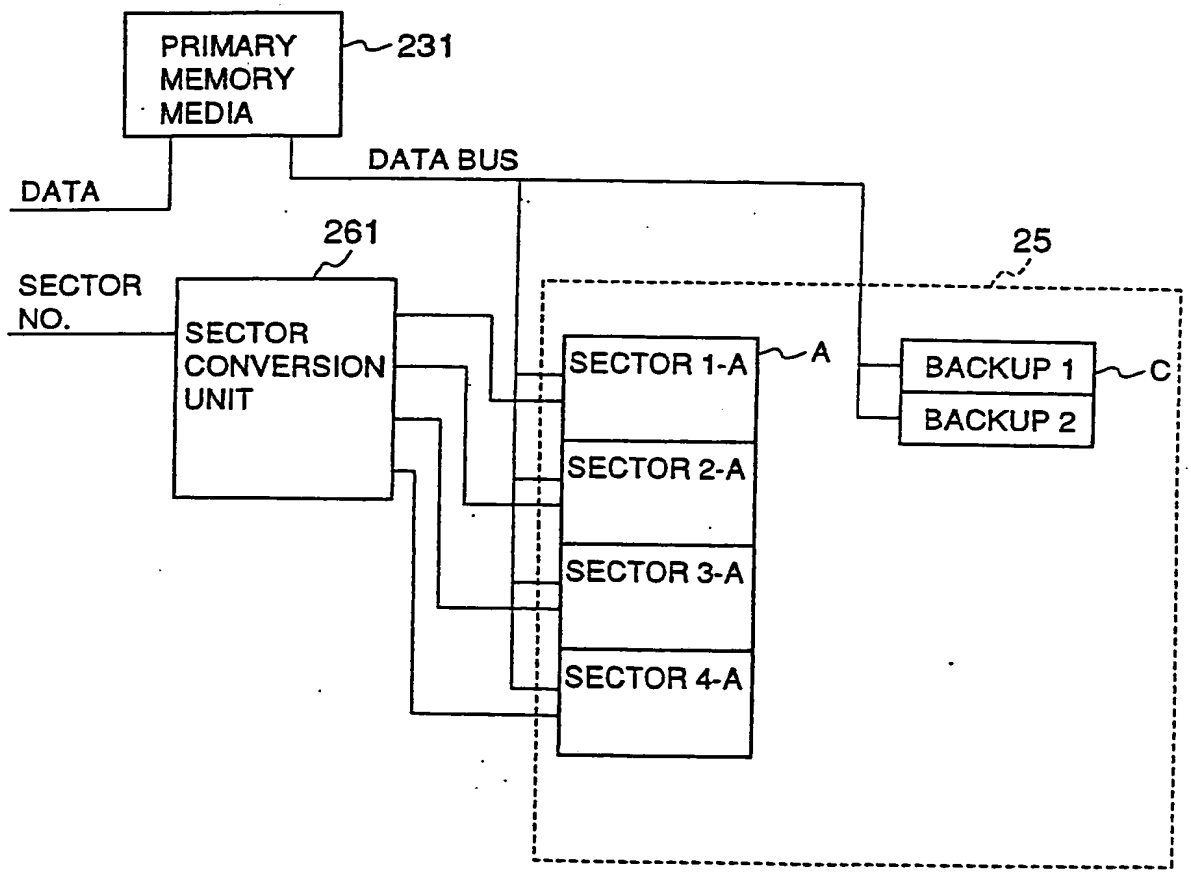

PRIMARY MEMORY MEDIA
231
DATA
DATA BUS
261
25
SECTOR NO.
SECTOR CONVERSION UNIT
SECTOR 1-A
A
SECTOR 2-A
SECTOR 3-A
SECTOR 4-A
BACKUP 1
BACKUP 2
C

FIG.20B

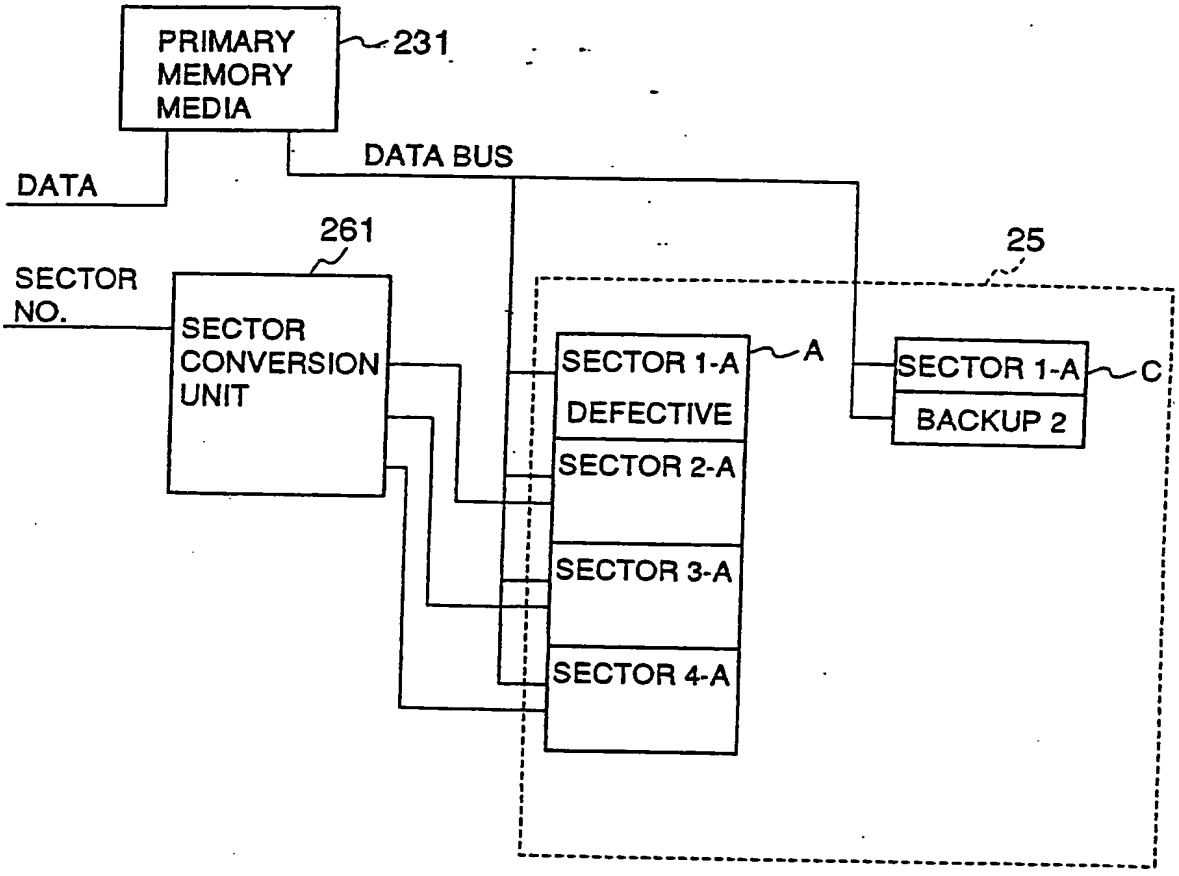

PRIMARY MEMORY MEDIA
231
DATA
DATA BUS
261
SECTOR NO.
SECTOR CONVERSION UNIT
25
SECTOR 1-A
A
DEFECTIVE
SECTOR 2-A
SECTOR 3-A
SECTOR 4-A
SECTOR 1-A
C
BACKUP 2

FIG.21A

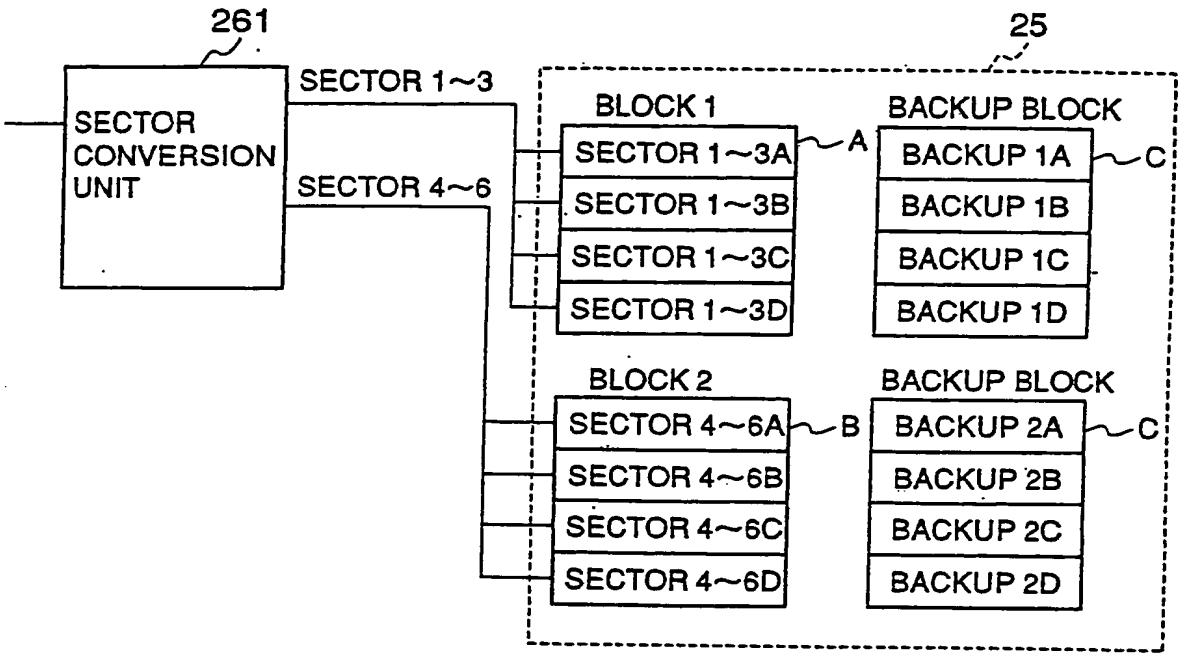

261
SECTOR CONVERSION UNIT
SECTOR 1~3
SECTOR 4~6
25
BLOCK 1
SECTOR 1~3A
SECTOR 1~3B
SECTOR 1~3C
SECTOR 1~3D
A
BACKUP BLOCK
BACKUP 1A
BACKUP 1B
BACKUP 1C
BACKUP 1D
C
BLOCK 2
SECTOR 4~6A
SECTOR 4~6B
SECTOR 4~6C
SECTOR 4~6D
B
BACKUP BLOCK
BACKUP 2A
BACKUP 2B
BACKUP 2C
BACKUP 2D
C

FIG.21B

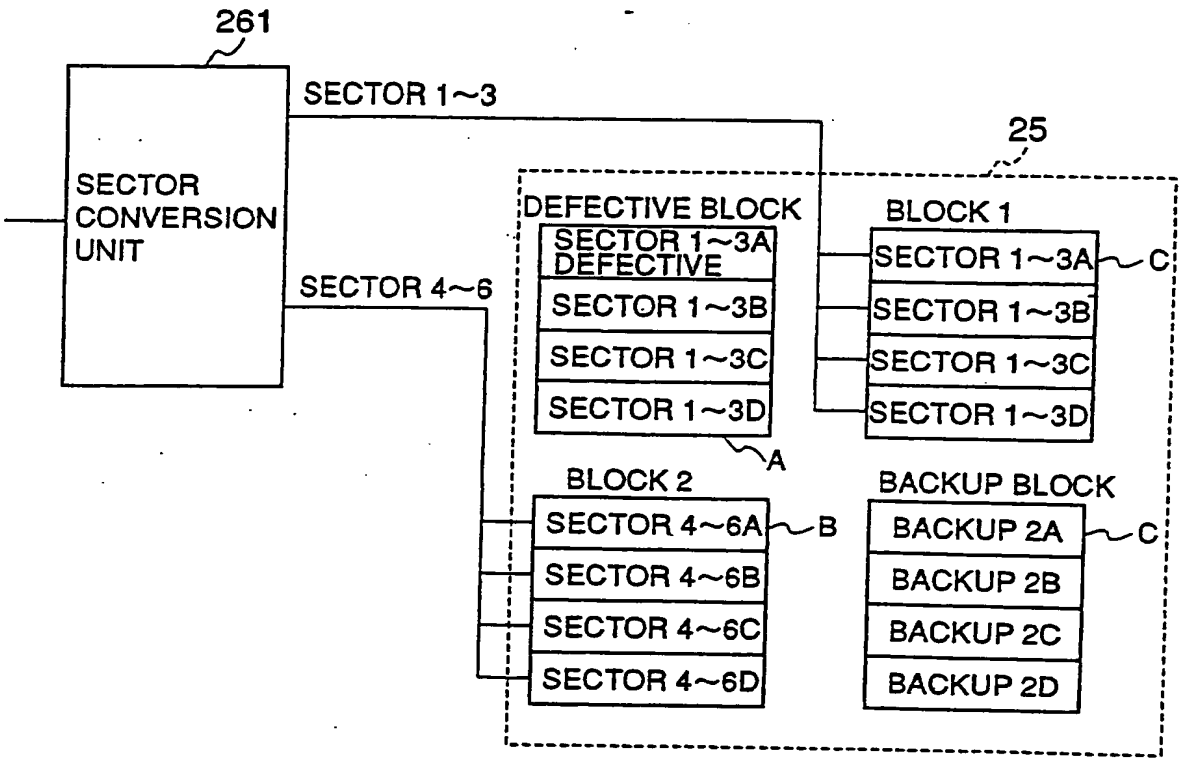

261
SECTOR CONVERSION UNIT
SECTOR 1~3
SECTOR 4~6
25
DEFECTIVE BLOCK
SECTOR 1~3A DEFECTIVE
SECTOR 1~3B
SECTOR 1~3C
SECTOR 1~3D
A
BLOCK 1
SECTOR 1~3A
SECTOR 1~3B
SECTOR 1~3C
SECTOR 1~3D
C
BLOCK 2
SECTOR 4~6A
SECTOR 4~6B
SECTOR 4~6C
SECTOR 4~6D
B
BACKUP BLOCK
BACKUP 2A
BACKUP 2B
BACKUP 2C
BACKUP 2D
C

FIG.22A

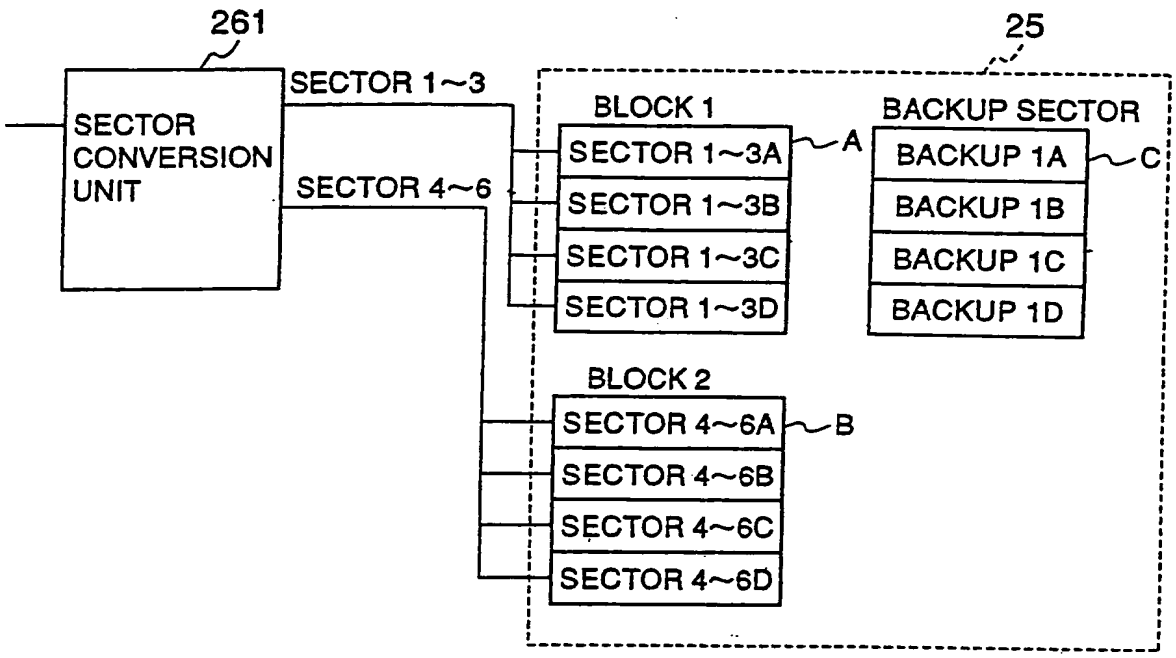

261
25
SECTOR CONVERSION UNIT
SECTOR 1~3
SECTOR 4~6
BLOCK 1
SECTOR 1~3A
SECTOR 1~3B
SECTOR 1~3C
SECTOR 1~3D
A
BACKUP SECTOR
BACKUP 1A
BACKUP 1B
BACKUP 1C
BACKUP 1D
C
BLOCK 2
SECTOR 4~6A
SECTOR 4~6B
SECTOR 4~6C
SECTOR 4~6D
B

FIG.22B

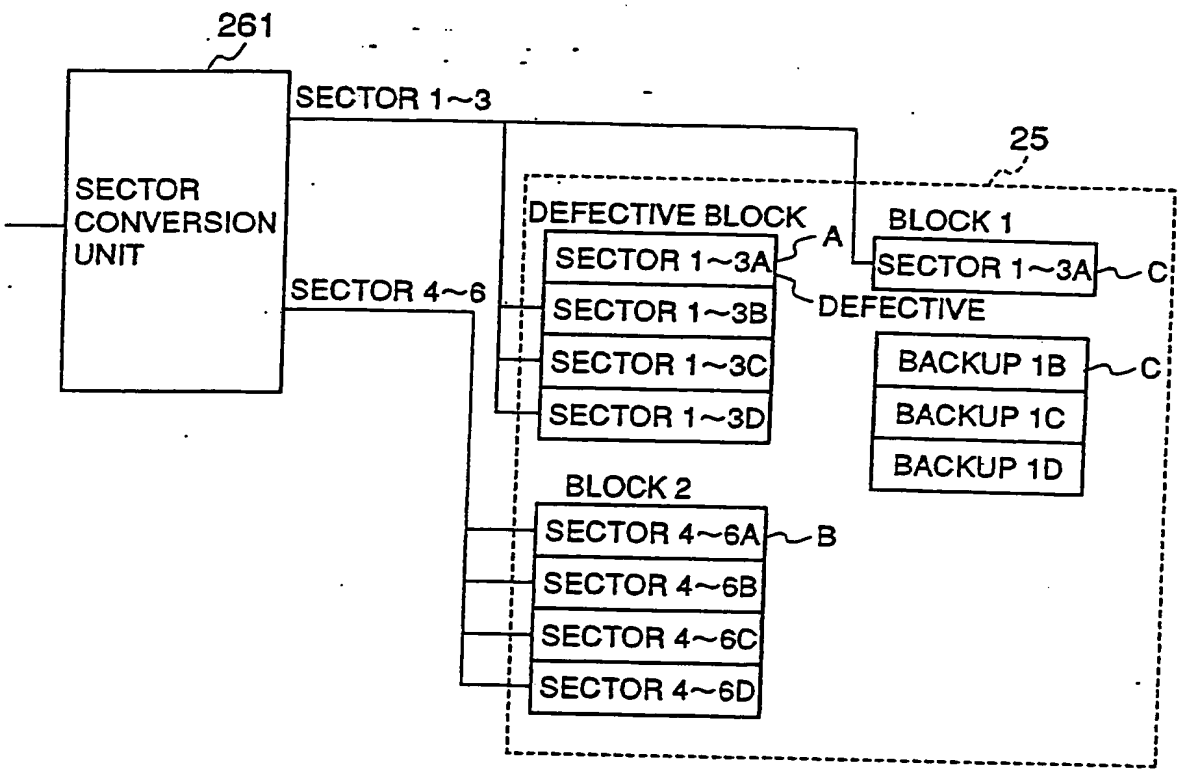

261
SECTOR 1~3
SECTOR CONVERSION UNIT
SECTOR 4~6
25
DEFECTIVE BLOCK
SECTOR 1~3A
A
SECTOR 1~3B
SECTOR 1~3C
SECTOR 1~3D
DEFECTIVE
BLOCK 1
SECTOR 1~3A
C
BACKUP 1B
C
BACKUP 1C
BACKUP 1D
BLOCK 2
SECTOR 4~6A
B
SECTOR 4~6B
SECTOR 4~6C
SECTOR 4~6D

FIG.23A

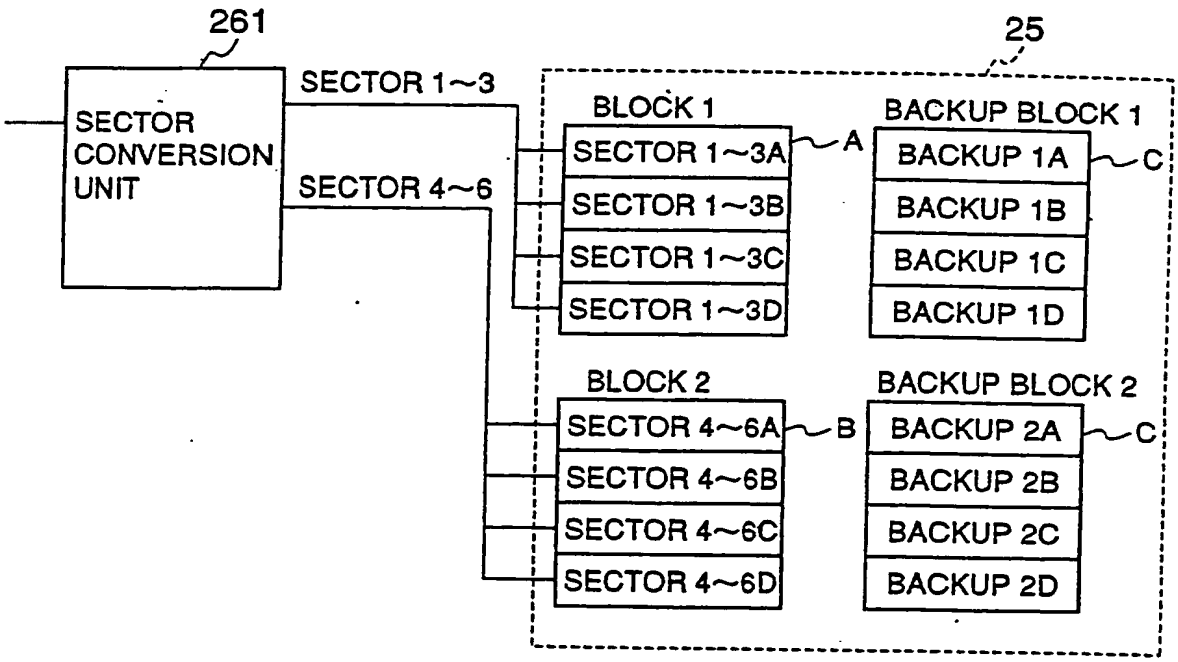

261
SECTOR CONVERSION UNIT
SECTOR 1~3
SECTOR 4~6
25
BLOCK 1
SECTOR 1~3A
SECTOR 1~3B
SECTOR 1~3C
SECTOR 1~3D
A
BACKUP BLOCK 1
BACKUP 1A
BACKUP 1B
BACKUP 1C
BACKUP 1D
C
BLOCK 2
SECTOR 4~6A
SECTOR 4~6B
SECTOR 4~6C
SECTOR 4~6D
B
BACKUP BLOCK 2
BACKUP 2A
BACKUP 2B
BACKUP 2C
BACKUP 2D
C

FIG.23B

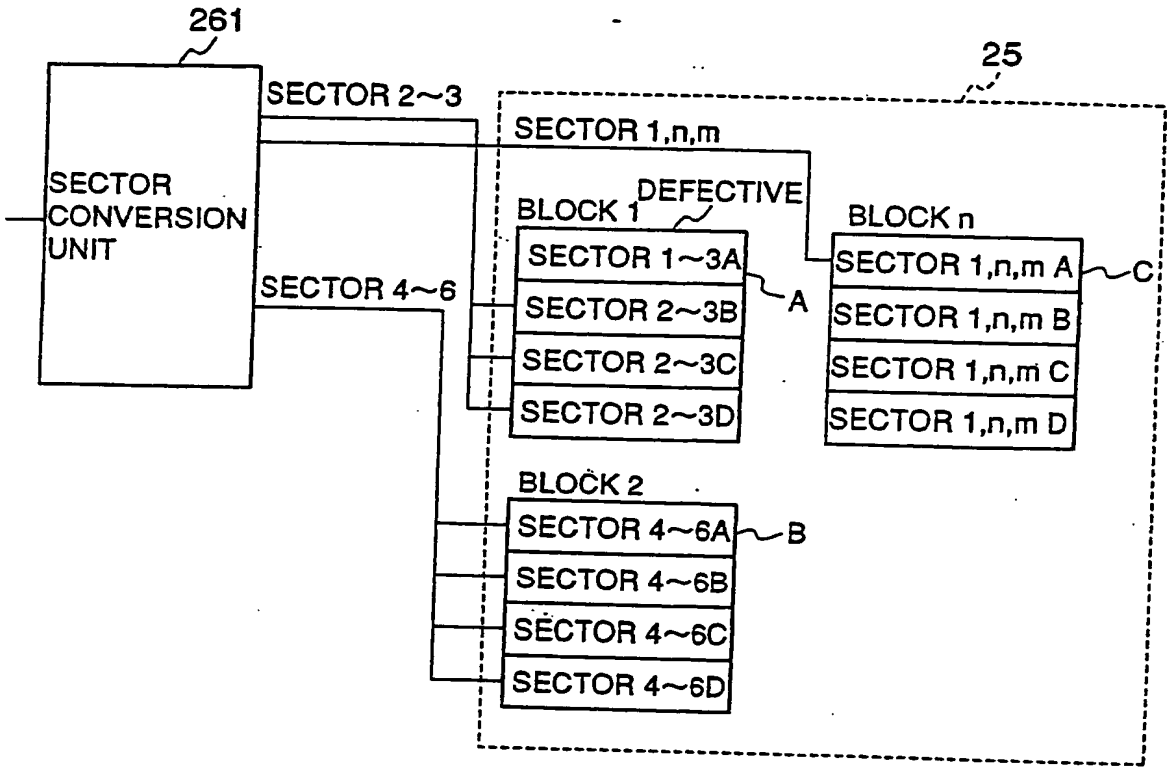

261
SECTOR CONVERSION UNIT
SECTOR 2~3
SECTOR 4~6
25
SECTOR 1,n,m
DEFECTIVE
BLOCK 1
SECTOR 1~3A
SECTOR 2~3B
SECTOR 2~3C
SECTOR 2~3D
A
BLOCK n
SECTOR 1,n,m A
SECTOR 1,n,m B
SECTOR 1,n,m C
SECTOR 1,n,m D
C
BLOCK 2
SECTOR 4~6A
SECTOR 4~6B
SECTOR 4~6C
SECTOR 4~6D
B

FIG.24A

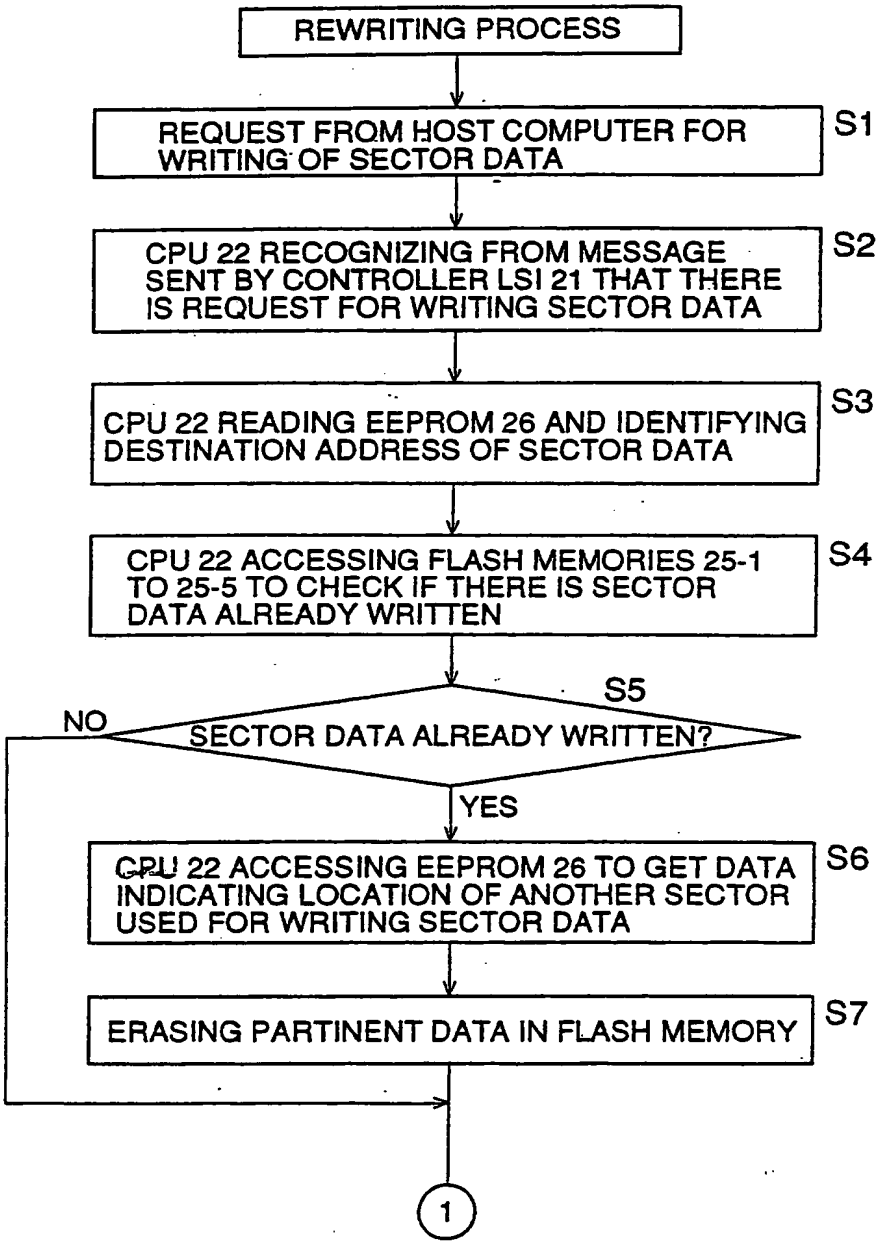

REWRITING PROCESS
REQUEST FROM HOST COMPUTER FOR WRITING OF SECTOR DATA
S1
CPU 22 RECOGNIZING FROM MESSAGE SENT BY CONTROLLER LSI 21 THAT THERE IS REQUEST FOR WRITING SECTOR DATA
S2
CPU 22 READING EEPROM 26 AND IDENTIFYING DESTINATION ADDRESS OF SECTOR DATA
S3
CPU 22 ACCESSING FLASH MEMORIES 25-1 TO 25-5 TO CHECK IF THERE IS SECTOR DATA ALREADY WRITTEN
S4
S5
SECTOR DATA ALREADY WRITTEN?
NO
YES
CPU 22 ACCESSING EEPROM 26 TO GET DATA INDICATING LOCATION OF ANOTHER SECTOR USED FOR WRITING SECTOR DATA
S6
ERASING PARTINENT DATA IN FLASH MEMORY
S7
1

FIG.24B

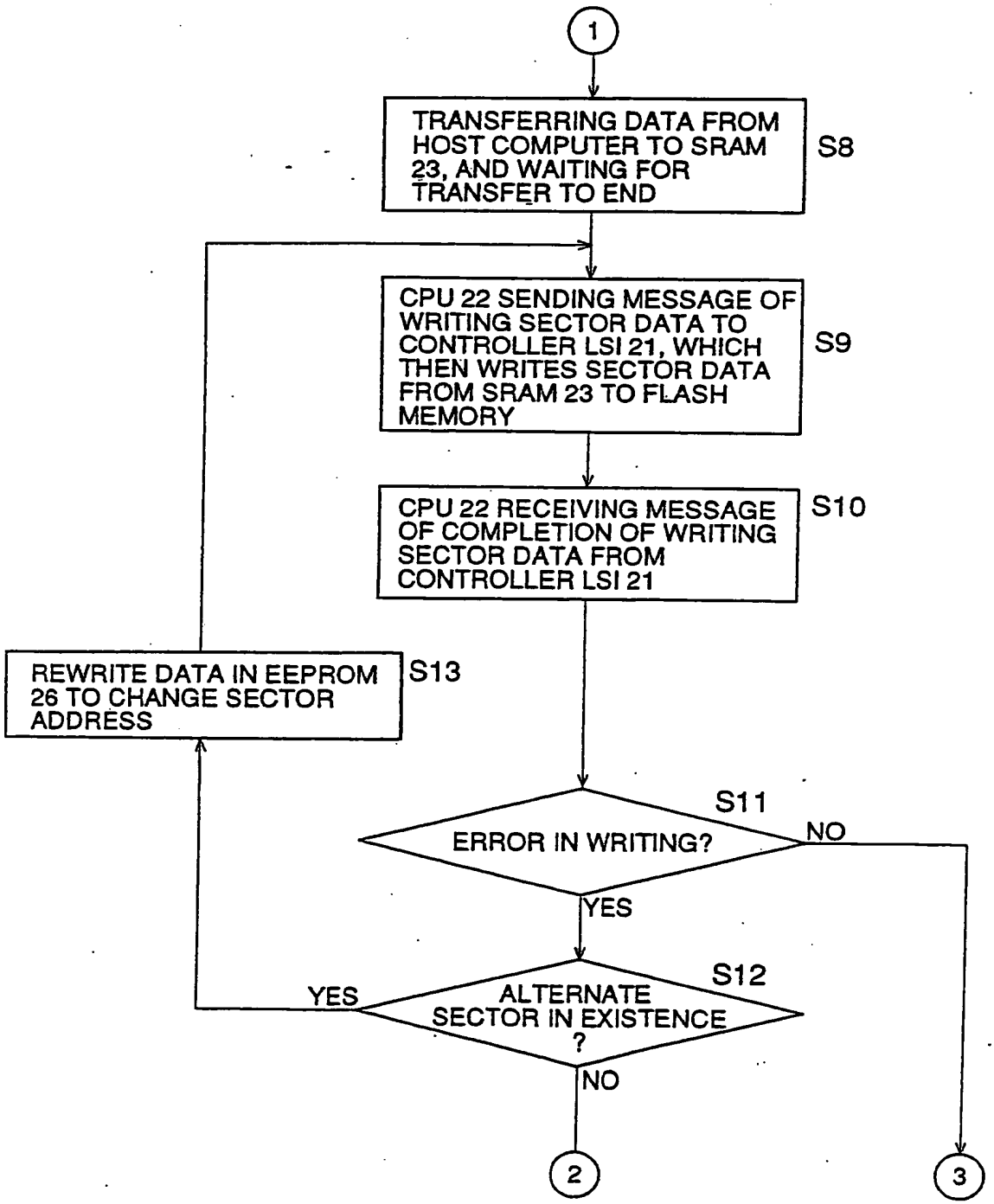

1
TRANSFERRING DATA FROM HOST COMPUTER TO SRAM 23, AND WAITING FOR TRANSFER TO END
S8
CPU 22 SENDING MESSAGE OF WRITING SECTOR DATA TO CONTROLLER LSI 21, WHICH THEN WRITES SECTOR DATA FROM SRAM 23 TO FLASH MEMORY
S9
CPU 22 RECEIVING MESSAGE OF COMPLETION OF WRITING SECTOR DATA FROM CONTROLLER LSI 21
S10
REWRITE DATA IN EEPROM 26 TO CHANGE SECTOR ADDRESS
S13
S11
ERROR IN WRITING?
NO
YES
S12
YES
ALTERNATE SECTOR IN EXISTENCE ?
NO
2
3

FIG.24C

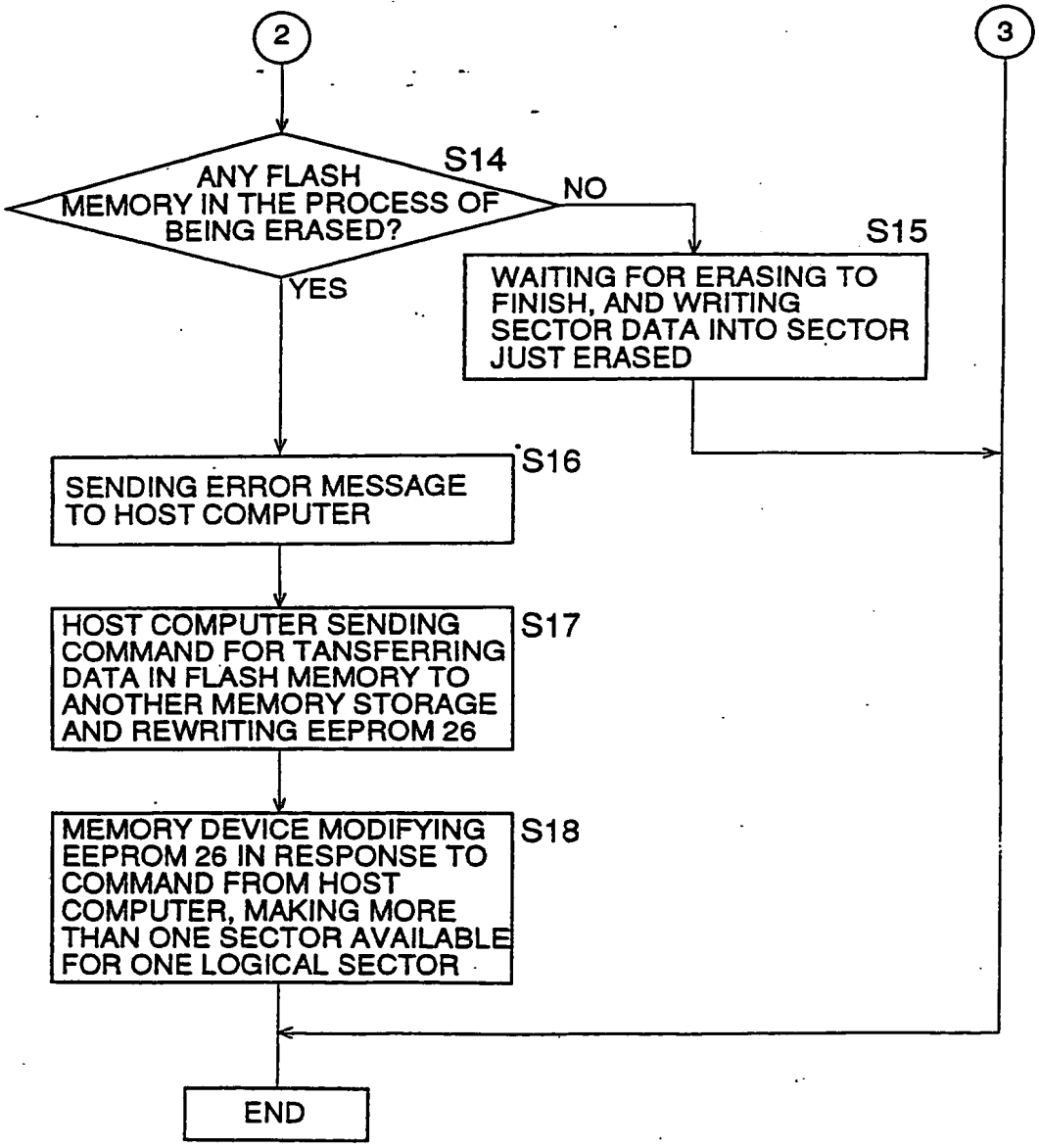

2
3
S14
ANY FLASH MEMORY IN THE PROCESS OF BEING ERASED?
NO
YES
S15
WAITING FOR ERASING TO FINISH, AND WRITING SECTOR DATA INTO SECTOR JUST ERASED
S16
SENDING ERROR MESSAGE TO HOST COMPUTER
S17
HOST COMPUTER SENDING COMMAND FOR TANSFERRING DATA IN FLASH MEMORY TO ANOTHER MEMORY STORAGE AND REWRITING EEPROM 26
S18
MEMORY DEVICE MODIFYING EEPROM 26 IN RESPONSE TO COMMAND FROM HOST COMPUTER, MAKING MORE THAN ONE SECTOR AVAILABLE FOR ONE LOGICAL SECTOR
END

FIG.25A

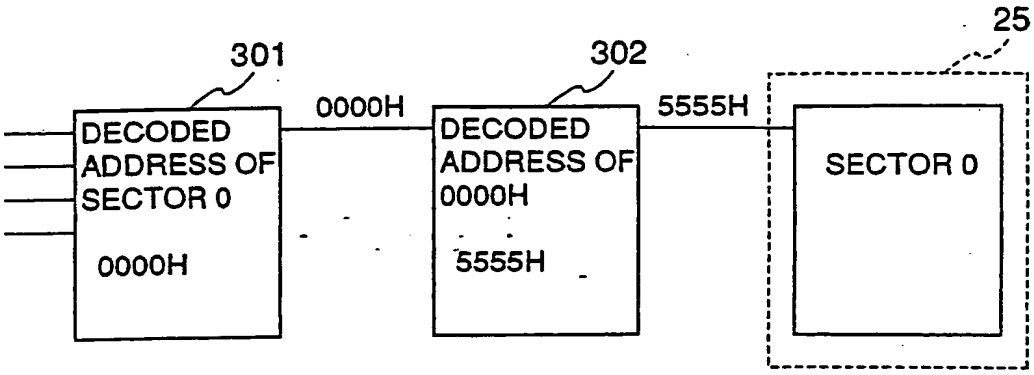


FIG.25B

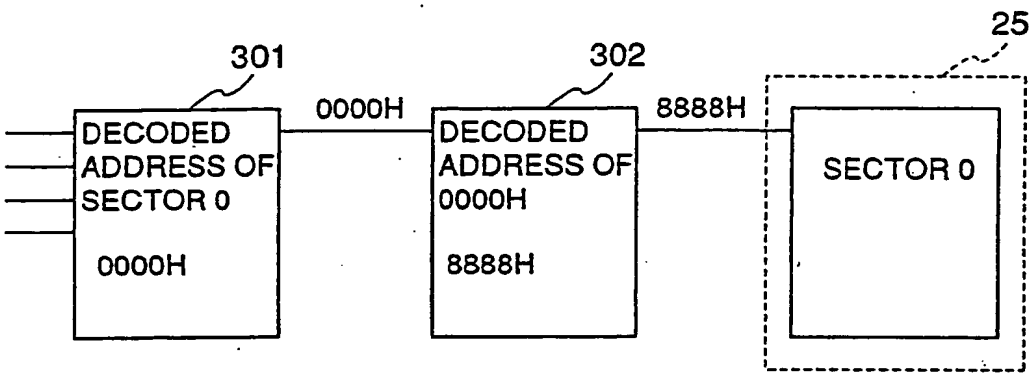


FIG.25C

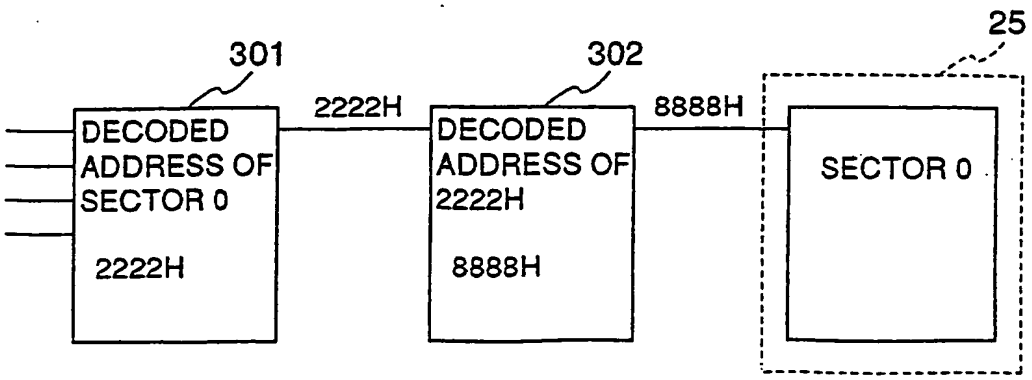


FIG.26

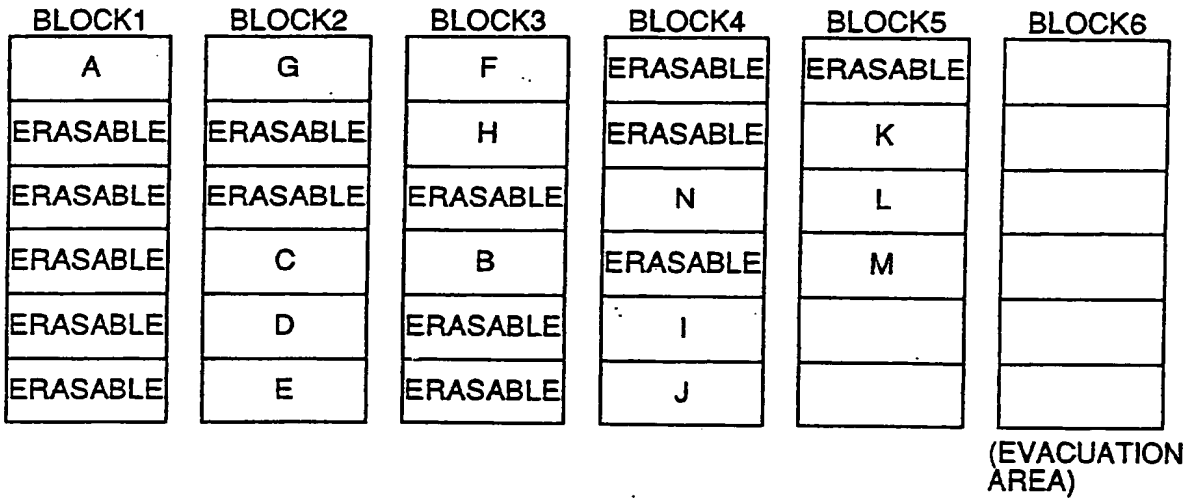

BLOCK1
A
ERASABLE
ERASABLE
ERASABLE
ERASABLE
ERASABLE
BLOCK2
G
ERASABLE
ERASABLE
C
D
E
BLOCK3
F
H
ERASABLE
B
ERASABLE
ERASABLE
BLOCK4
ERASABLE
ERASABLE
N
ERASABLE
I
J
BLOCK5
ERASABLE
K
L
M
BLOCK6
(EVACUATION AREA)

FIG.27

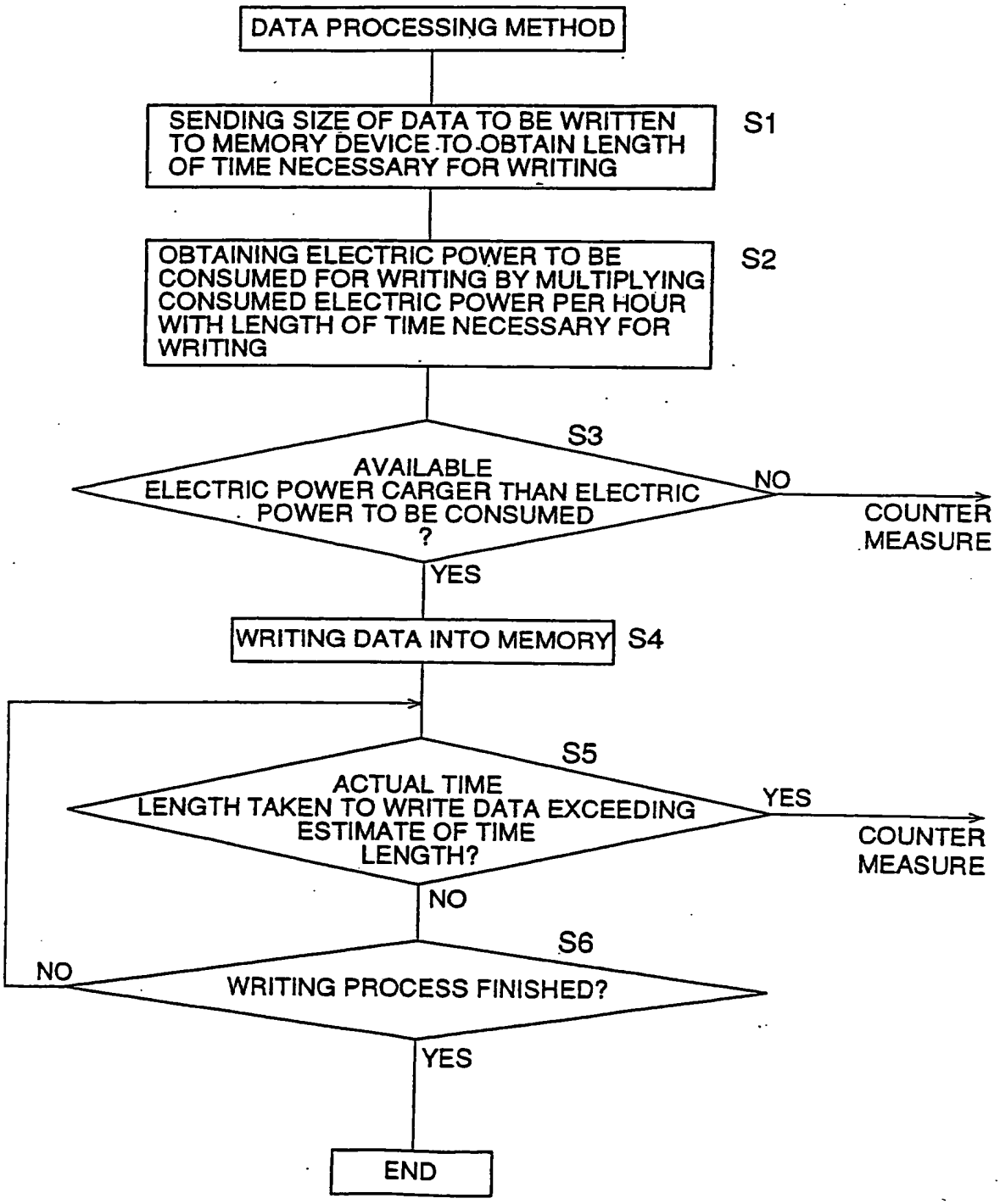

DATA PROCESSING METHOD
SENDING SIZE OF DATA TO BE WRITTEN TO MEMORY DEVICE TO OBTAIN LENGTH OF TIME NECESSARY FOR WRITING
S1
OBTAINING ELECTRIC POWER TO BE CONSUMED FOR WRITING BY MULTIPLYING CONSUMED ELECTRIC POWER PER HOUR WITH LENGTH OF TIME NECESSARY FOR WRITING
S2
S3
AVAILABLE ELECTRIC POWER CARGER THAN ELECTRIC POWER TO BE CONSUMED ?
NO
COUNTER MEASURE
YES
WRITING DATA INTO MEMORY
S4
S5
ACTUAL TIME LENGTH TAKEN TO WRITE DATA EXCEEDING ESTIMATE OF TIME LENGTH?
YES
COUNTER MEASURE
NO
S6
NO
WRITING PROCESS FINISHED?
YES
END

FIG.28A

FIG.28B

FIG.28C

	b4	b0	OUTPUT
1	0	0	0
2	0	1	0
3	1	0	0
4	1	1	1

b0 OF PERMANENT HIGH LEVEL

b4 OF PERMANENT HIGH LEVEL

FIG.29A

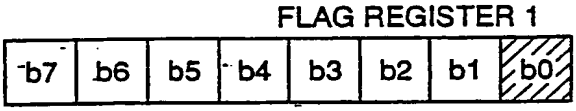


FIG.29B

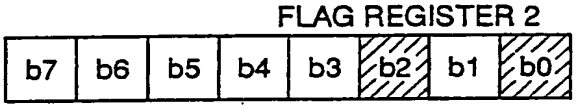


FIG.29C

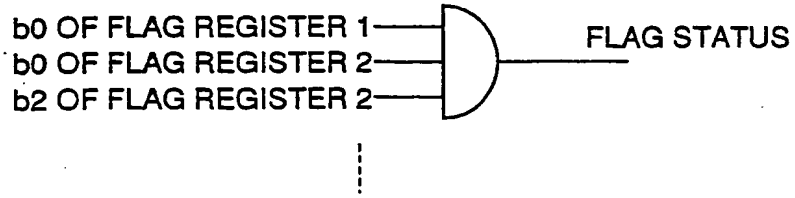


FIG.30

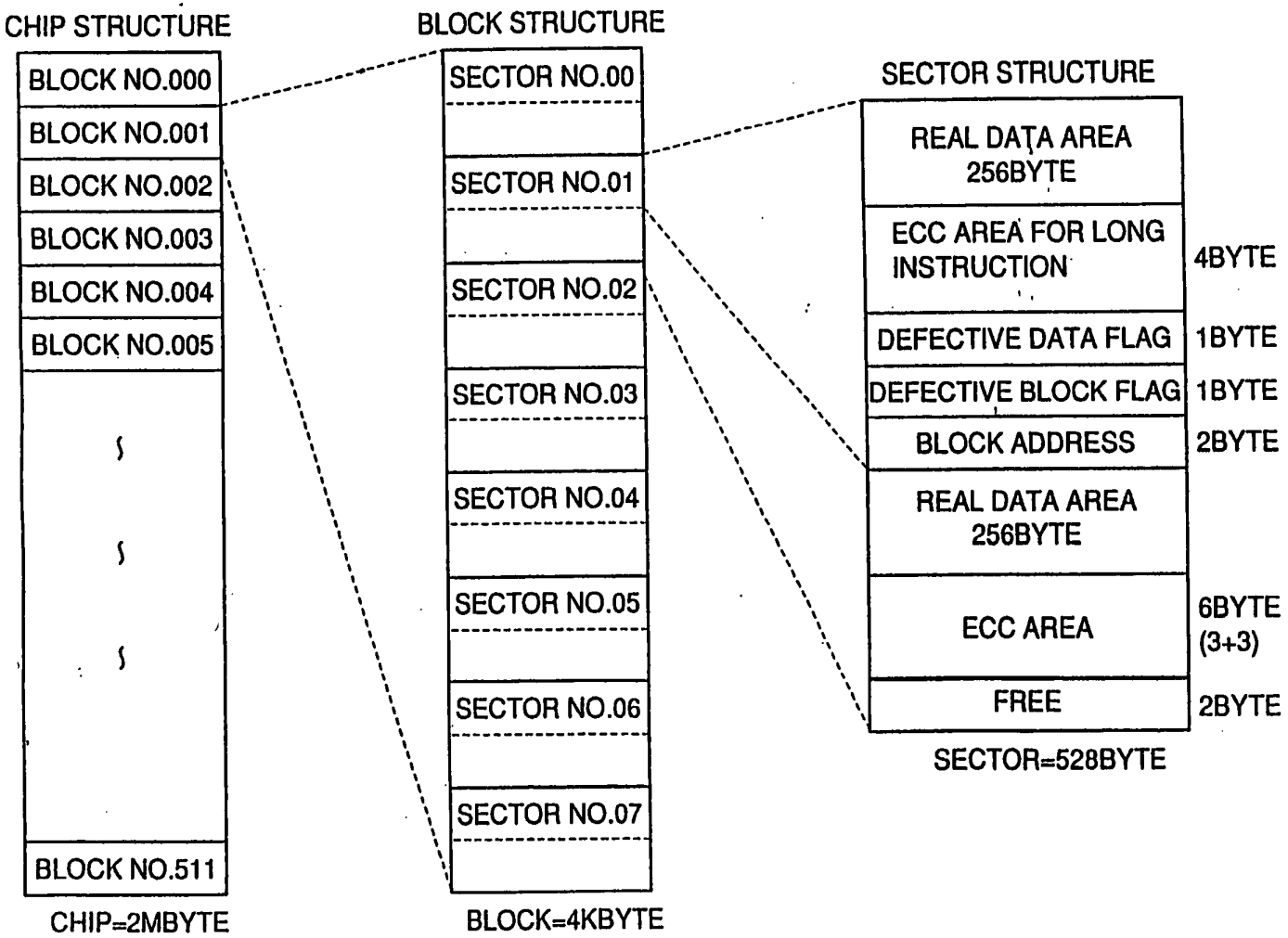

CHIP STRUCTURE
BLOCK NO.000
BLOCK NO.001
BLOCK NO.002
BLOCK NO.003
BLOCK NO.004
BLOCK NO.005
BLOCK NO.511
CHIP=2MBYTE
BLOCK STRUCTURE
SECTOR NO.00
SECTOR NO.01
SECTOR NO.02
SECTOR NO.03
SECTOR NO.04
SECTOR NO.05
SECTOR NO.06
SECTOR NO.07
BLOCK=4KBYTE
SECTOR STRUCTURE
REAL DATA AREA 256BYTE
ECC AREA FOR LONG INSTRUCTION
4BYTE
DEFECTIVE DATA FLAG
1BYTE
DEFECTIVE BLOCK FLAG
1BYTE
BLOCK ADDRESS
2BYTE
REAL DATA AREA 256BYTE
ECC AREA
6BYTE (3+3)
FREE
2BYTE
SECTOR=528BYTE

FIG.31A

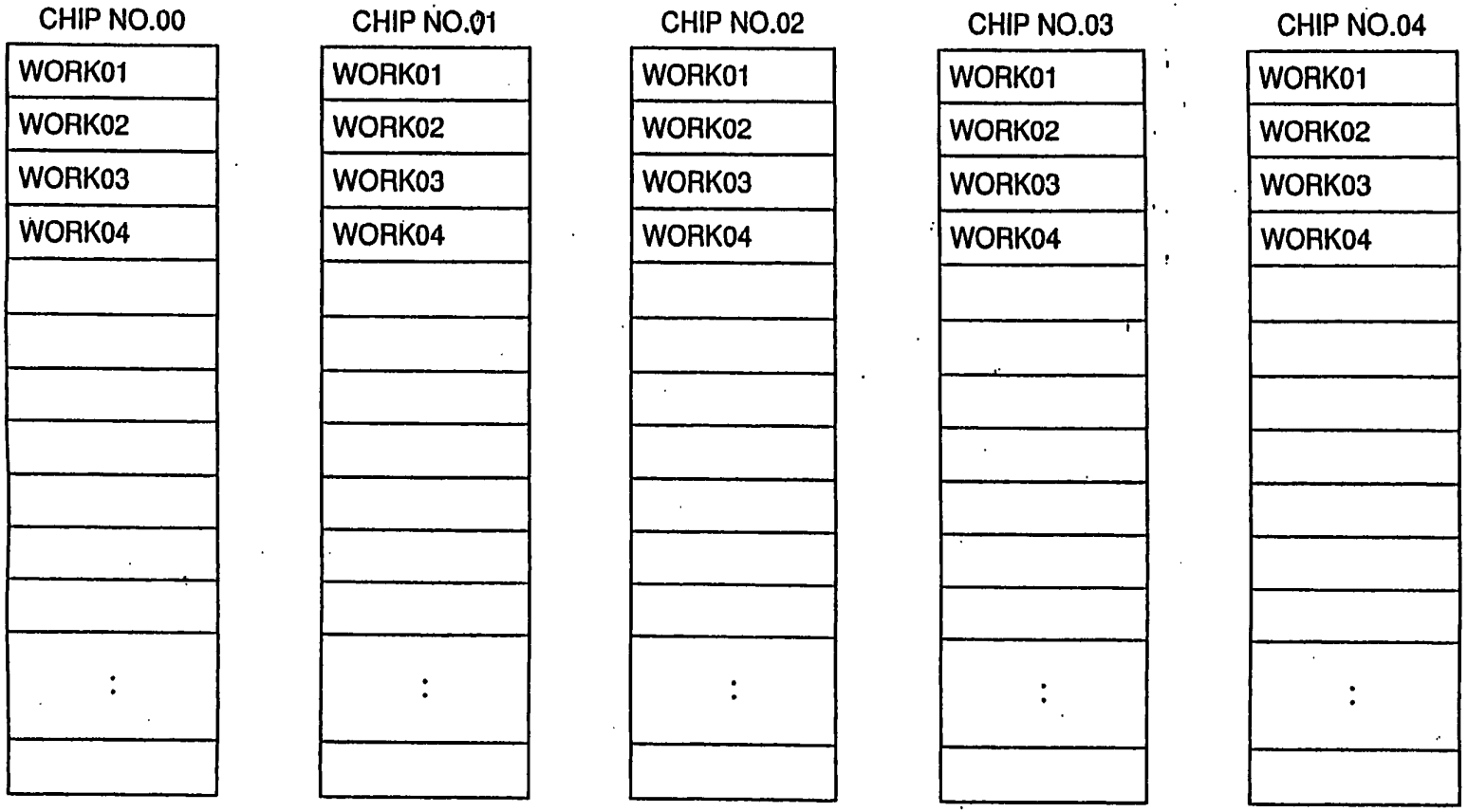

CHIP NO.00
WORK01
WORK02
WORK03
WORK04
CHIP NO.01
WORK01
WORK02
WORK03
WORK04
CHIP NO.02
WORK01
WORK02
WORK03
WORK04
CHIP NO.03
WORK01
WORK02
WORK03
WORK04
CHIP NO.04
WORK01
WORK02
WORK03
WORK04

FIG.31B

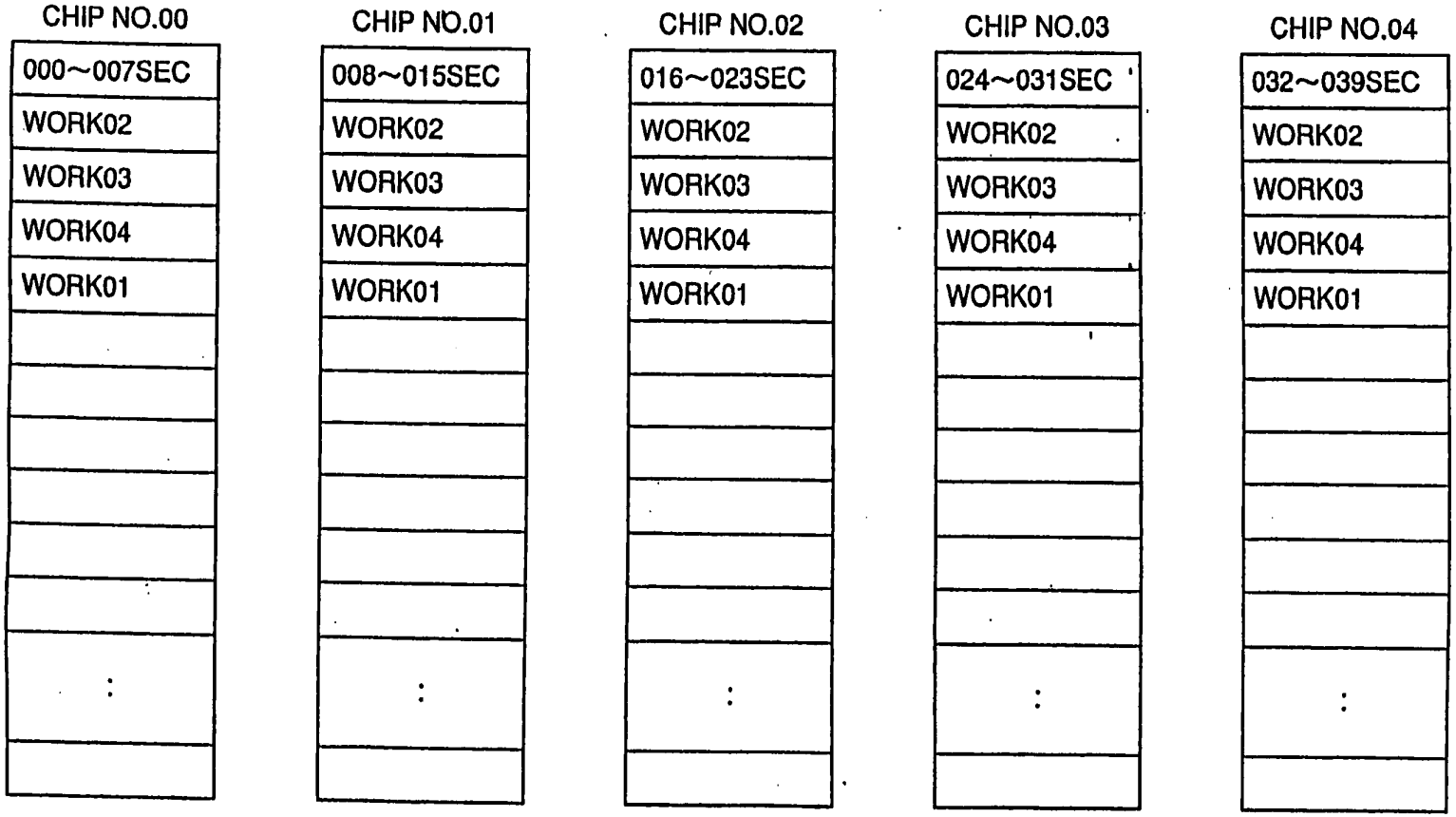

CHIP NO.00
000~007SEC
WORK02
WORK03
WORK04
WORK01
CHIP NO.01
008~015SEC
WORK02
WORK03
WORK04
WORK01
CHIP NO.02
016~023SEC
WORK02
WORK03
WORK04
WORK01
CHIP NO.03
024~031SEC
WORK02
WORK03
WORK04
WORK01
CHIP NO.04
032~039SEC
WORK02
WORK03
WORK04
WORK01

FIG.31C

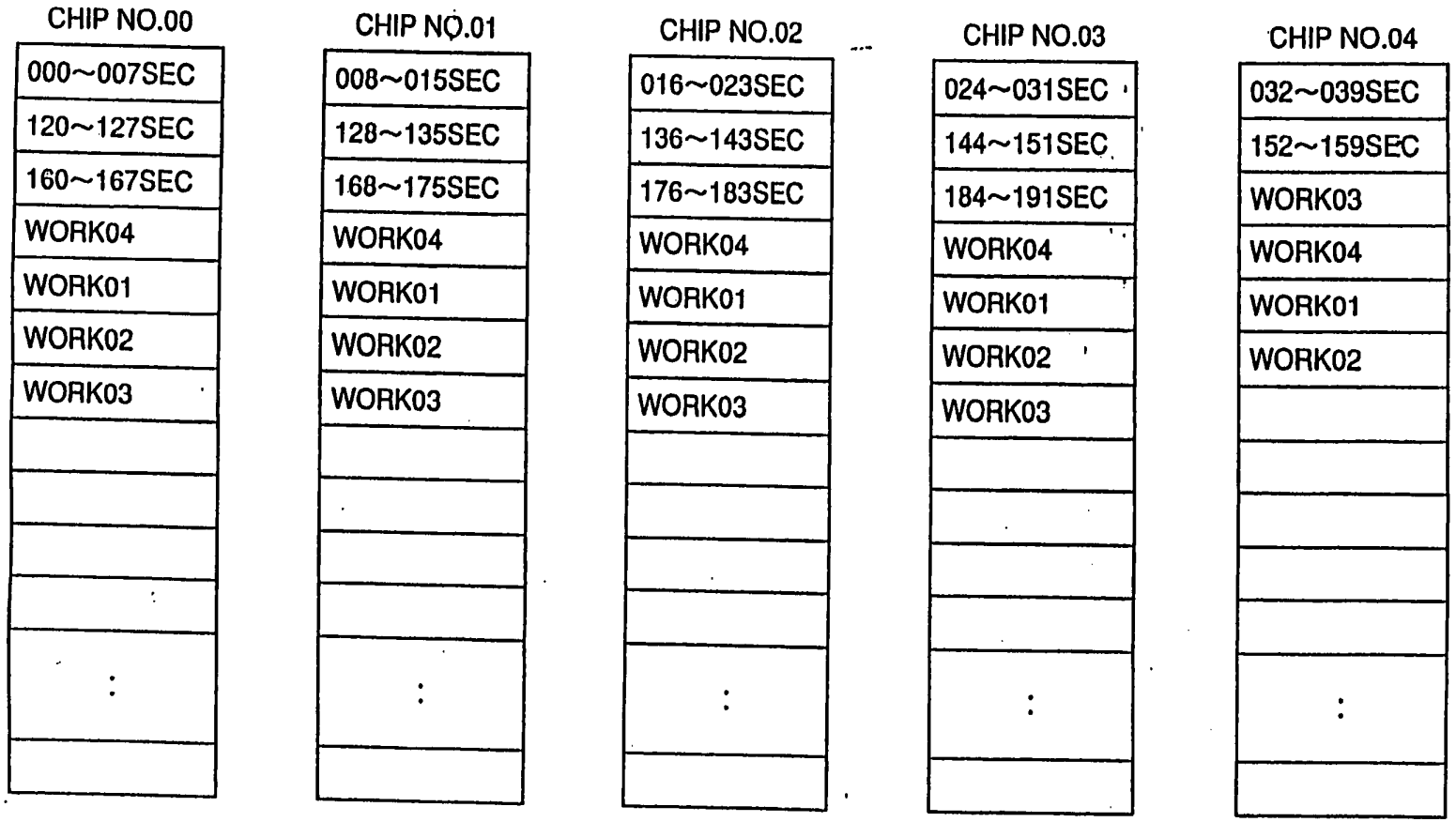

CHIP NO.00
000~007SEC
120~127SEC
160~167SEC
WORK04
WORK01
WORK02
WORK03
CHIP NO.01
008~015SEC
128~135SEC
168~175SEC
WORK04
WORK01
WORK02
WORK03
CHIP NO.02
016~023SEC
136~143SEC
176~183SEC
WORK04
WORK01
WORK02
WORK03
CHIP NO.03
024~031SEC
144~151SEC
184~191SEC
WORK04
WORK01
WORK02
WORK03
CHIP NO.04
032~039SEC
152~159SEC
WORK03
WORK04
WORK01
WORK02

FIG.31D

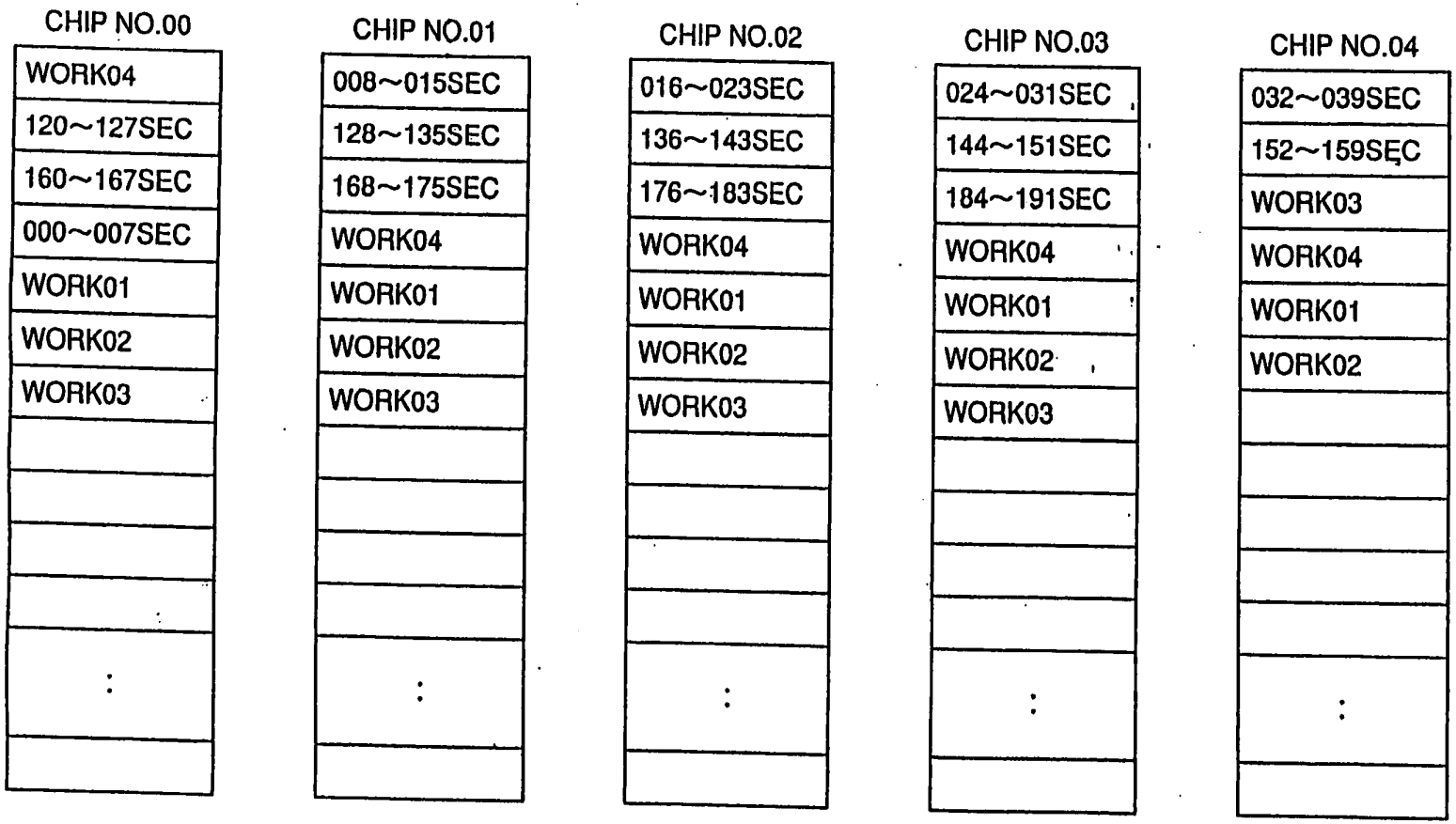
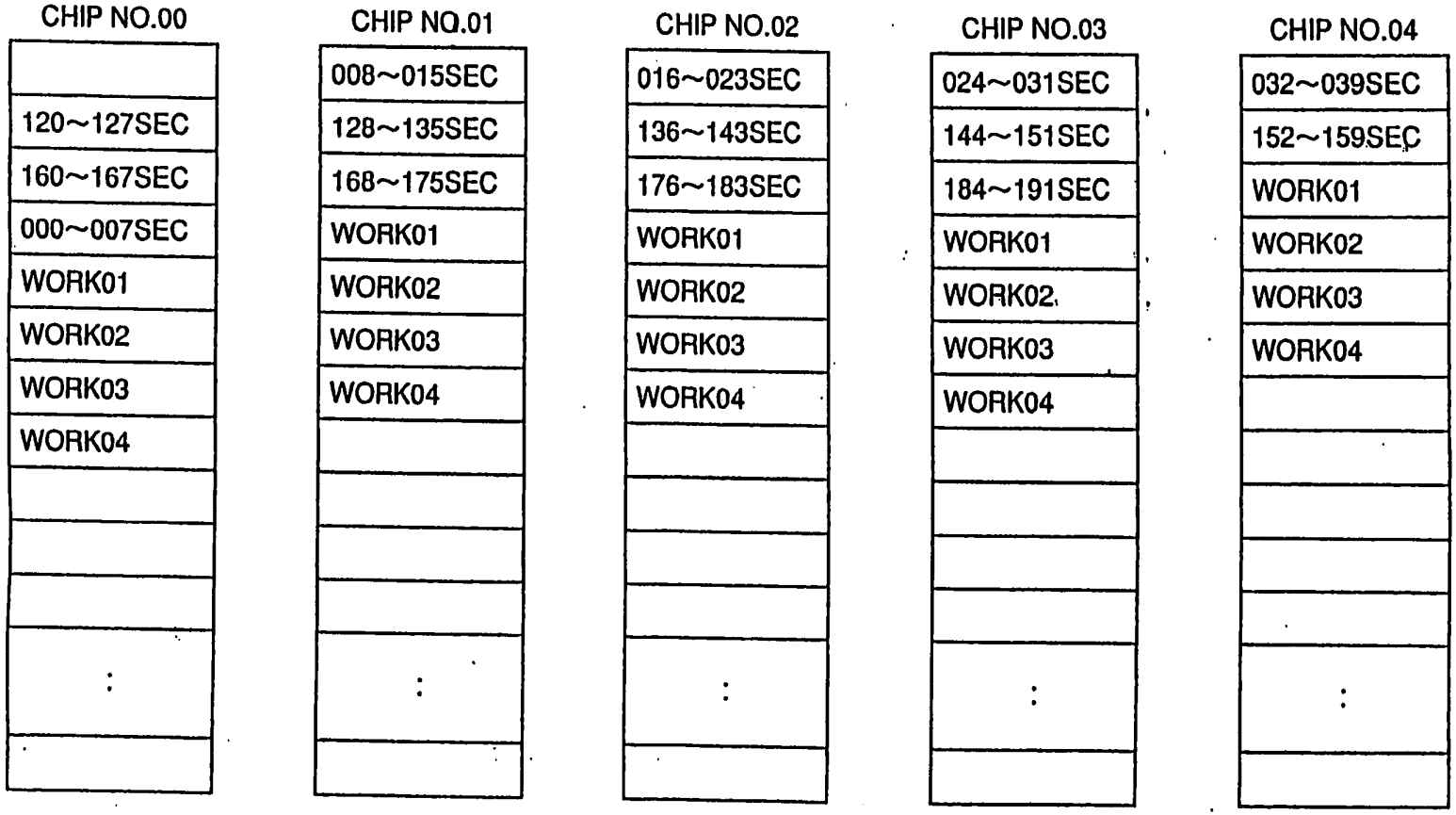

CHIP NO.00
WORK04
120~127SEC
160~167SEC
000~007SEC
WORK01
WORK02
WORK03
CHIP NO.01
008~015SEC
128~135SEC
168~175SEC
WORK04
WORK01
WORK02
WORK03
CHIP NO.02
016~023SEC
136~143SEC
176~183SEC
WORK04
WORK01
WORK02
WORK03
CHIP NO.03
024~031SEC
144~151SEC
184~191SEC
WORK04
WORK01
WORK02
WORK03
CHIP NO.04
032~039SEC
152~159SEC
WORK03
WORK04
WORK01
WORK02

FIG.31E


CHIP NO.00
120~127SEC
160~167SEC
000~007SEC
WORK01
WORK02
WORK03
WORK04
CHIP NO.01
008~015SEC
128~135SEC
168~175SEC
WORK01
WORK02
WORK03
WORK04
CHIP NO.02
016~023SEC
136~143SEC
176~183SEC
WORK01
WORK02
WORK03
WORK04
CHIP NO.03
024~031SEC
144~151SEC
184~191SEC
WORK01
WORK02
WORK03
WORK04
CHIP NO.04
032~039SEC
152~159SEC
WORK01
WORK02
WORK03
WORK04